This set of VLSI Multiple Choice Questions & Answers (MCQs) focuses on “Basic MOS Transistors-1”.

1. Electronics are characterized by
   a) low cost b) low weight and volume c) reliability d) all of the mentioned
   Answer: d
   Explanation: Electronics are characterized by reliability, low power dissipation, extremely low weight and volume, low cost, can cope up with high degree of sophistication and complexity.
2. Speed power product is measured as the product of
   a) gate switching delay and gate power dissipation b) gate switching delay and gate power absorption c) gate switching delay and net gate power d) gate power dissipation and absorption
   Answer: a
   Explanation: Speed power product is measure in picojoules and it is the product of gate switching delay and gate power dissipation.
3. nMOS devices are formed in
   a) p-type substrate of high doping level b) n-type substrate of low doping level c) p-type substrate of moderate doping level d) n-type substrate of high doping level
   Answer: c
   Explanation: nMOS devices are formed in a p-type substrate of moderate doping level. nMOS devices have higher mobility and is cheaper.
4. Source and drain in nMOS device are isolated by
   a) a single diode b) two diodes c) three diodes d) four diode
   Answer: b
   Explanation: The source and drain regions are formed by diffusing n-type impurity, it gives rise to depletion region which extend in more lightly doped p-region. Thus Source and drain in a nMOS device are isolated by two diodes.
5. In depletion mode, source and drain are connected by
   a) insulating channel b) conducing channel c) Vdd d) Vss
   Answer: b
   Explanation: In depletion mode, source and drain are connected by conducting channel but the channel can be closed by applying suitable negative voltage to the gate.
6. The condition for non saturated region is
   a) Vds = Vgs – Vt b) Vgs lesser than Vt c) Vds lesser than Vgs – Vt d) Vds greater than Vgs – Vt
   Answer: c
   Explanation: The condition for non saturated region is Vds lesser Vgs – Vt. In non saturation region MOSFET acts as voltage source. Varying Vds will provide significant change in drain current.
7. In enhancement mode, device is in _____ condition
   a) conducting b) non conducting c) partially conducting d) insulating
   Answer: b
   Explanation: In enhancement mode, the decive is in non conducting condition. For n-type FET, thershold voltage is positive and p-type threshold voltage is negative.

8. The condition for non conducting mode is
   a) Vds lesser than Vgs b) Vgs lesser than Vds c) Vgs = Vds = 0 d) Vgs = Vds = Vs = 0
   Answer: d
   Explanation: In enhancement mode the device is in non conducting mode, and its condition is Vds = Vgs = Vs = 0.
9. nMOS is
   a) donor doped b) acceptor doped c) all of the mentioned d) none of the mentioned
   Answer: b
   Explanation: nMOS transistors are acceptor doped. Acceptor is a dopant which when added forms p-type region. Some of the accpetors are silicon, boron, aluminium etc.
10. MOS transistor structure is
    a) symmetrical b) non symmetrical c) semi symmetrical d) pseudo symmetrical
    Answer: a
    Explanation: MOS transistor structure is completely symmetrical with respect to source and drain.
11. pMOS is
    a) donor doped b) acceptor doped c) all of the mentioned d) none of the mentioned
    Answer: a
    Explanation: nMOS is acceptor doped and pMOS is donor doped devices. Acceptor doped forms p-type region and donor doped forms n-type region.
12. Inversion layer in enhancement mode consists of excess of
    a) positive carriers b) negative carriers c) both in equal quantity d) neutral carriers
    Answer: b
    Explanation: Inversion layer in enhancement mode consists of excess of negative carriers that is electron.
13. The condition for linear region is
    a) Vgs lesser than Vt b) Vgs greater than Vt c) Vds lesser than Vgs d) Vds greater than Vgs
    Answer: b
    Explanation: The condition for linear region is Vgs > Vt. The power of MOS in linear region is less. It is a power dissipating region.
14. As source drain voltage increases, channel depth
    a) increases b) decreases c) logarithmically increases d) exponentially increses
15. Answer: b
    Explanation: As source drain voltage Vds increases, the channel depth at the drain end decreases.
16. MOS transistors consists of
    a) semiconductor layer b) metal layer c) layer of silicon-di-oxide d) all of the mentioned
    Answer: d
    Explanation: MOS transistors is formed as a sandwich consisting of a semiconductor layer, a silicon-di-oxide layer and a metal layer.
17. In MOS transistors, _____ is used for their gate
    a) metal b) silicon-di-oxide c) polysilicon d) gallium
    Answer: c
    Explanation: In MOS transistors, polycrystalline silicon is used for their gate region instead of metal. Polysilicon gates have replaced all other older devices.

18. The gate region consists of
    a) insulating layer b) conducting layer c) lower metal layer d) p type layer
    Answer: b
    Explanation: The gate region is a sandwich consisting of semiconductor layer, an insulating layer and an upper metal layer.
19. Electrical charge flows from
    a) source to drain b) drain to source c) source to ground d) source to gate
    Answer: a
    Explanation: Electrical charge or current flows from source to drain depending on the charge applied to the gate region.
20. Source in MOS transistors is doped with _____ material
    a) n-type b) p-type c) n & p type d) none of the mentioned
21. Answer: a
    Explanation: Source and drain in the MOS transistors are doped with N-type material and substrate is doped with p-type material.
22. In N channel MOSFET which is the more negative of the elements?
    a) source b) gate c) drain d) source and drain
    Answer: a
    Explanation: In N channel MOSFET, source is the more negative of the elements and in the case of P channel MOSFET, it is the more positive of the elements.
23. If the gate is given sufficiently large charge, electrons will be attracted to
    a) drain region b) channel region c) switch region d) bulk region
    Answer: b
    Explanation: If the gate is given sufficiently large charge, the negative charge carreirs, electrons will be attracted from the bulk of the substrate material into the channel region below the oxide.
24. Enhancement mode device acts as ____ switch, depletion mode acts as _____ switch
    a) open, closed b) closed, open c) open, open d) close, close
    Answer: a
    Explanation: Enhancement mode transistor acts as open switch whereas depletion mode transistor acts as normally closed switch.
25. Depletion mode MOSFETs are more commonly used as
    a) switches b) resistors c) buffers d) capacitors
    Answer: b
    Explanation: Depletion mode MOSFETs are more commonly used as resistors than as switches. As permanently on switch it has high resistance.
26. Enhancement mode MOSFETs are more commonly used as
    a) switches b) resistors c) buffers d) capacitor
    Answer: a
    Explanation: Enhancement mode MOSFETs are more commonly used as switches and depletion mode devices are more used as resistors.
27. Depletion mode transistor should be large.
    a) true b) false
    Answer: a
    Explanation: Depletion mode transistors should be made large that is long and thin to create the large ‘on’ resistance.

28. Which expression is true?
    a) charging time < discharging time b) charging time > discharging time c) charging time = discharging time d) charging time and discharging time are not related
    Answer: b
    Explanation: When driving a capacitive output load, charging time will be long compared to the discharging time.
29. Overheating in device occurs due to less number of resistors per unit area.
    a) true b) false
    Answer: b
    Explanation: When the number of resistors per unit area increases, the device may not dissipate heat very well. This results in device overheating which leads to its failure.
30. In n channel MOSFET, _____ is constant
    a) channel length b) channel width c) channel depth d) channel concentration
    Answer: a
    Explanation: In all n channel MOSFET transistors, channel length is constant where as channel width can be varied.
31. VLSI technology uses _____ to form integrated circuit
    a) transistors b) switches c) diodes d) buffers
    Answer: a
    Explanation: Very-large scale integration is the process of creating integrated circuit with thousands of transistors into one single chip.
32. Medium scale integration has
    a) ten logic gates b) fifty logic gates c) hundred logic gates d) thousands logic gates
    Answer: c
    Explanation: Small scale integration has one or more logic gate. Further improved technology is medium scale integration which consists of hundred logic gates. Large scale integration has thousand logic gates.
33. The difficulty in achieving high doping concentration leads to
    a) error in concentration b) error in variation c) error in doping d) distrubution error
    Answer: b
    Explanation: As photolithography comes closer to fundamental law of optics, achieving high accuracy in doping concentration becomes difficult, which leads to error due to variation.
34. _____ is used to deal with effect of variation
    a) chip level technique b) logic level technique c) switch level technique d) system level technique
    Answer: d
    Explanation: Designers must simulate multiple fabrication process or use system level technique for dealing with effects of variation.
35. As die size shrinks, the complexity of making the photomasks
    a) increases b) decreases c) remains the same d) cannot be determined
    Answer: a
    Explanation: As the die size shrinks due to scaling, the number of die per wafer increases and the complexity of making the photomasks increases rapidly.
36. _____ architecture is used to design VLSI
    a) system on a device b) single open circuit c) system on a chip d) system on a circuit

Answer: c
Explanation: SoC that is system on a chip architecture is used to design the very high level integrated circuit.

37. The design flow of VLSI system is
    1. architecture design 2. market requirement 3. logic design 4. HDL coding
    a) 2-1-3-4 b) 4-1-3-2 c) 3-2-1-4 d) 1-2-3-4
    Answer: a
    Explanation: The order of the design flow of VLSI circuit is market requirement, architecture design, logic design, HDL coding and then verification.
38. _____ is used in logic design of VLSI
    a) LIFO b) FIFO c) FILO d) LILO
    Answer: b
    Explanation: First in first out (FIFO) technique and finite state machine technique is used in the logic design of the VLSI circuits.
39. Which provides higher integration density?
    a) switch transistor logic b) transistor buffer logic c) transistor transistor logic d) circuit level logic
    Answer: c
    Explanation: Transistor-transistor logic offers higher integration density and it became the first integrated circuit revolution.
40. Physical and electrical specification is given in
    a) architectural design b) logic design c) system design d) functional design
    Answer: d
    Explanation: Functional design defines the major functional units of the system, interconnections, physical and electrical specifications.
41. Which is the high level representation of VLSI design
    a) problem statement b) logic design c) HDL program d) functional design
    Answer: a
    Explanation: Problem statement is a high level representation of the system. Performance, functionality and physical dimensions are considered here.
42. Gate minimization technique is used to simplify the logic.
    a) true b) falsw
    Answer: a
    Explanation: Gate minimization technique is used to find the simplest, smallest and effective implementation of the logic.
43. VLSI technology uses _____ to form integrated circuit
    a) transistors b) switches c) diodes d) buffers
    Answer: a
    Explanation: Very-large scale integration is the process of creating integrated circuit with thousands of transistors into one single chip.
44. Medium scale integration has
    a) ten logic gates b) fifty logic gates c) hundred logic gates d) thousands logic gates
    Answer: c
    Explanation: Small scale integration has one or more logic gate. Further improved technology is medium scale integration which consists of hundred logic gates. Large scale integration has thousand logic gates.

45. The difficulty in achieving high doping concentration leads to
    a) error in concentration b) error in variation c) error in doping d) distrubution error
    Answer: b
    Explanation: As photolithography comes closer to fundamental law of optics, achieving high accuracy in doping concentration becomes difficult, which leads to error due to variation.
46. _____ is used to deal with effect of variation
    a) chip level technique b) logic level technique c) switch level technique d) system level technique
    Answer: d
    Explanation: Designers must simulate multiple fabrication process or use system level technique for dealing with effects of variation.
47. As die size shrinks, the complexity of making the photomasks
    a) increases b) decreases c) remains the same d) cannot be determined
    Answer: a
    Explanation: As the die size shrinks due to scaling, the number of die per wafer increases and the complexity of making the photomasks increases rapidly.
48. _____ architecture is used to design VLSI
    a) system on a device b) single open circuit c) system on a chip d) system on a circuit
    Answer: c
    Explanation: SoC that is system on a chip architecture is used to design the very high level integrated circuit.
49. The design flow of VLSI system is
    1. architecture design 2. market requirement 3. logic design 4. HDL coding
    a) 2-1-3-4 b) 4-1-3-2 c) 3-2-1-4 d) 1-2-3-4
    Answer: a
    Explanation: The order of the design flow of VLSI circuit is market requirement, architecture design, logic design, HDL coding and then verification.
50. _____ is used in logic design of VLSI
    a) LIFO b) FIFO c) FILO d) LILO
    Answer: b
    Explanation: First in first out (FIFO) technique and finite state machine technique is used in the logic design of the VLSI circuits.
51. Which provides higher integration density?
    a) switch transistor logic b) transistor buffer logic c) transistor transistor logic d) circuit level logic
    Answer: c
    Explanation: Transistor-transistor logic offers higher integration density and it became the first integrated circuit revolution.
52. Physical and electrical specification is given in
    a) architectural design b) logic design c) system design d) functional design
    Answer: d
    Explanation: Functional design defines the major functional units of the system, interconnections, physical and electrical specifications.
53. Which is the high level representation of VLSI design
    a) problem statement b) logic design c) HDL program d) functional design

Answer: a
Explanation: Problem statement is a high level representation of the system. Performance, functionality and physical dimensions are considered here.

54. Gate minimization technique is used to simplify the logic.
a) true b) false
Answer: a
Explanation: Gate minimization technique is used to find the simplest, smallest and effective implementation of the logic.

55. nMOS fabrication process is carried out in
a) thin wafer of a single crystal b) thin wafer of multiple crystals c) thick wafer of a single crystal d) thick wafer of multiple crystals
Answer: a
Explanation: nMOS fabrication process is carried out in thin wafer of a single crystal with high purity.

56. _____ impurities are added to the wafer of the crystal
a) n impurities b) p impurities c) siicon d) crystal
Answer: b
Explanation: p impurities are introduced as the crystal is grown. This increases the hole concentration in the device.

57. What kind of substrate is provided above the barrier to dopants?
a) insulating b) conducting c) silicon d) semi conducting
Answer: a
Explanation: Above a layer of silicon dioxide which acts as barrier, insulating layer is provided upon which other layers may be deposited and patterned.

58. The photoresist layer is exposed to
a) visible light b) ultraviolet light c) infra red light d) LED
Answer: b
Explanation: The photoresist layer is exposed to ultraviolet light to mark the regions where diffusion is to take place.

59. In nMOS device, gate material could be
a) silicon b) polysilicon c) boron d) phosphorus
Answer: b
Explanation: In nMOS device, the gate material could be metal or polysilicon. This polysilicon layer has heavily doped polysilicon deposited by CVD.

60. The commonly used bulk substrate in nMOS fabrication is
a) silicon crystal b) silicon-on-sapphire c) phosphorus d) silicon-di-oxide
Answer: c
Explanation: In nMOS fabrication, the bulk substrate used can be either bulk silicon or silicon-on-sapphire.

61. In nMOS fabrication, etching is done using
a) plasma b) hydrochloric acid c) sulphuric acid d) sodium chloride
Answer: a
Explanation: In nMOS fabrication, etching is done using hydroflouric acid or plasma. Etching is a process used to remove layers from the surface.

62. Heavily doped polysilicon is deposited using
a) chemical vapour decomposition b) chemical vapour deposition c) chemical deposition d) dry deposition
Answer: b
Explanation: The polysilicon layer consists of heavily doped polysilicon deposited by chemical vapour deposition.

Propogation Delays".

1. Propogation time is directly proportional to
a) x
b) 1/x
c) x^2
d) $1/x^2$
View Answer

Answer: c
Explanation: Propogation time is directly proportional to square of the propogation distance (x^2). It is the time taken by the signal to move from input port to output port.

2. The total resistance can be given as
a) nRs
b) nrRs
c) rRs
d) Rs
View Answer

Answer: b
Explanation: The total resistance can be given as the product of nrRs where r is the relative resistance per section in terms of Rs.

3. Total capacitance can be given as
a) n(square Cg)
b) nc(square Cg)
c) c(square Cg)
d) square Cg
View Answer

Answer: b
Explanation: Total capacitance can be given as the product of nc(square Cg) where c is the relative capacitance per section in terms of square Cg.

4. Overall delay is directly proportional to
a) n
b) 1/n
c) n^2

d) $1/n^2$
View Answer

Answer: c
Explanation: The overall delay is directly proportional to n^2 , where n is the number of pass transistors in series.

5. The number of pass transistors connected in series can be increased if
a) compressor is connected
b) buffer is connected
c) ground is connected
d) voltage regulator is connected
View Answer

Answer: b
Explanation: The number of pass transistors connected in series can be increased by connecting buffer in between.

6. Buffer is used because
a) it increases the speed
b) decreases senstivity to noise
c) decreases speed
d) does not affect speed
View Answer

Answer: a
Explanation: Buffer is used for long polysilicon runs because it increses the speed and reduces the sensitivity to noise.

7. The overall delay is _____ to the relative resistance r
a) directly proportional
b) inversely proportional
c) exponentially proportional
d) not dependent
View Answer

Answer: a
Explanation: The overall delay is directly proportional to the relative resistance r. Overall delay is given as product of n^2rcƮ.

8. Small disturbances of noise
a) decreases the inverter voltage
b) increases the output voltage
c) switches the inverter stage between 0 to 1
d) does not switch the stage and keeps it stable
View Answer

Answer: c
Explanation: Small disturbanes of noise switches the inverter stage between 0 and 1 or vice versa. It disturbs the normal operation or behaviour.

9. The buffer speeds up the
a) rise time
b) fall time
c) all of the mentioned
d) none of the mentioned
View Answer

Answer: a
Explanation: The buffer speeds up the rise time of propogated signal edge. A buffer is the combination of two inverters in which one output is fed to the other as the input.

10. Overall delay increases as n
a) increases
b) decreases
c) exponentially decreases
d) logarithmically decreases
View Answer

Answer: a
Explanation: Overall delay increases as n increases where n is the number of pass transistors connected in series.

1. Which contribute to the wiring capacitance?
a) fringing fields
b) interlayer capacitance
c) peripheral capacitance
d) all of the mentioned
View Answer

Answer: d
Explanation: The sources of capacitances which contribute to the total wiring capacitance are fringing field capacitance, interlayer capacitance and peripheral capacitance.

2. What does the value d in fringing field capacitance measures?
a) thickness of wire
b) length of the wire
c) wire to substrate separation
d) wire to wire separation
View Answer

Answer: c
Explanation: The quantity d in fringing field capacitance measures the wire to substrate separation. It is the distance between the wire and the substrate used in the device.

3. Total wire capacitance is equal to
a) area capacitance
b) fringing field capacitance
c) area capacitance + fringing field capacitance
d) peripheral capacitance
View Answer

Answer: c
Explanation: Total wire capacitance can be given as the sum of area capacitance and fringing field capacitance.

4. Interlayer capacitance occurs due to
a) separation between plates
b) electric field between plates
c) charges between plates
d) parallel plate effect
View Answer

Answer: d
Explanation: Interlayer capacitance occurs due to parallel plate effect between one layer and another. When one capacitance value comes closer to another they create some combined effects.

5. Which capacitance must be higher?
a) metal to polysilicon capacitance
b) metal to substrate capacitance
c) metal to metal capacitance
d) diffusion capacitance
View Answer

Answer: a
Explanation: Metal to polysilicon capacitance should be higher than metal to substrate capacitance. This is due to that when one layer underlies the other and in consequence interlayer capacitance is highly dependent on layout.

6. Peripheral capacitance is given in _____ eper unit length
a) nano farad
b) pico farad
c) micro farad
d) farad
View Answer

Answer: b
Explanation: Peripheral capacitance is given in picofarads per unit length. This is the sidewall capacitance. Each diode has this side wall capacitance.

7. For greater relative value of peripheral capacitance, _____ should be small
a) source area
b) drain area
c) both of the mentioned
d) none of the mentioned
View Answer

Answer: c
Explanation: The smaller the source or drain area, the greater the relative value of peripheral capacitance as they are both inversely related.

8. Diffusion capacitance is equal to
a) area capacitance
b) peripheral capacitance
c) fringing field capacitance
d) area capacitance + peripheral capacitance
View Answer

Answer: d
Explanation: Diffusion capacitance is given by the sum of area capacitance and peripheral capacitance.

9. Polysilicon is suitable for
a) small distance
b) large distance
c) all of the mentioned'
d) none of the mentioned
View Answer

Answer: a
Explanation: Polysilicon is unsuitable for routing Vdd or Vss other than for very small distance because of the relatively high Rs value of the polysilicon layer.

10. Which has high voltage drop?
a) metal layer
b) polysilicon layer
c) diffusion layer
d) silicide layer
View Answer

Answer: b
Explanation: Polysilicon layer has high voltage drop. It has moderate RC product.

11. Which layer has high capacitance value?
a) metal
b) diffusion
c) silicide
d) polysilicon
View Answer

Answer: b
Explanation: Diffusion or active layer has high capacitance value due to which it has low or moderate IR drop.

12. Which layer has high resistance value?
a) polysilicon
b) silicide
c) diffusion
d) metal
View Answer

Answer: a
Explanation: Polysilicon layer has high resistance value and due to this it has high IR drop.

13. While measuring the output load capacitance Cgs,n and Cgs,p is not considered. Why?
a) Because Cgs,n and Cgs,p are the capacitances at the input nodes.
b) Because Cgs,n and Cgs,p does not exist during the operation of CMOS inverter
c) Because Cgs,n and Cgs,p are storing opposite charges and cancel out each other during calculation of load capacitance
d) None of the mentioned
View Answer

Answer: a
Explanation: Cgs,n and Cgs,p are gate to source capacitances of nMOS and pMOS transistors in CMOS inverter. They are measured at input node. Therefore they are not considered for calculation of load capacitance.

14. During the calculation of load capacitance of a 1st stage CMOS inverter, the input node capacitances, Cgs,n and Cgs,p of the 2nd stage CMOS inverter is also considered.
a) True
b) False
View Answer

Answer: b
Explanation: Instead thin oxide capacitance over the gate area is used for calculation.

1. Conducting layer is separated from substrate using
a) dielectric layer
b) silicon layer

c) metal layer
d) diffusion layer
View Answer

Answer: a
Explanation: Conducting layer is separated from the substrate by using dielectric or insulating layer as both are electrical insulators that can be polarized by an applied electric field.

2. Gate to channel capacitance of 5 micron technology is _____ pF X $10^{(-4)}$ $(micrometer)^2$.
a) 1
b) 2
c) 4
d) 0.4
View Answer

Answer: c
Explanation: Gate to channel capacitance of 5 micron technology is 4 pF X $10^{(-4)}$ $(micrometer)^2$. It is the standard typical calculated value.

3. Area capacitance of diffusion region of 2 micron technology is _____ pF X $10^{(-4)}$ $(micrometer)^2$.
a) 2
b) 2.75
c) 3.75
d) 4.75
View Answer

Answer: c
Explanation: Area capacitane of diffusion region of 2 micron technology is 3.75 pF X $10^{(-4)}$ $(micrometer)^2$.

4. Relative capacitance of diffusion region of 5 micron technology is
a) 1
b) 0.25
c) 1.25
d) 2
View Answer

Answer: b
Explanation: The relative capacitance of diffusion region of 5 micron technology is 0.25. The relative value is calculated by comparing two values of same type.

5. A feature size square has
a) L > W
b) W > L
c) L = W

d) L > d
View Answer

Answer: c
Explanation: A feature size square has L = W and its gate to channel capacitance value is called as square Cg.

6. The standard square Cg value of a 5 micron technology is
a) 0.01 pF
b) 0.1 pF
c) 1 pF
d) 10 pF
View Answer

Answer: a
Explanation: The standard square Cg value of a 5 micron technology is 0.01 pF. This standard square Cg value can be calculated by using the area of standard square value and the capacitance value.

7. The standard square Cg value of a 1.2 micron technology is
a) 0.01 pF
b) 0.0023 pF
c) 0.023 pF
d) 0.23 pF
View Answer

Answer: b
Explanation: The standard square Cg value of a 1.2 micron technology is 0.0023 pF.

8. Relative area for L = 20λ and W = 3λ is
a) 10
b) 15
c) 1/15
d) 1/10
View Answer

Answer: b
Explanation: Relative area for L = 20λ and W = 3λ is = (20λ X 3λ) / (2λ X 2λ) = 15. Relative area has no unit as two quantities of same type have been used.

9. The value of gate capacitance is
a) 0.25 square Cg
b) 1 square Cg
c) 1.25 square Cg
d) 1.5 square Cg
View Answer

Answer: b
Explanation: The value of gate capacitance is one square Cg. This is the standard value.

10. Delay unit of 5 micron technology is
a) 1 nsec
b) 0.1 nsec
c) 0.01 nsec
d) 1 sec
View Answer

Answer: b
Explanation: Delay unit of 5 micron technology is 0.1 nsec.

11. Delay unit of 1.2 micron technology is
a) 0.064 nsec
b) 0.0064 nsec
c) 0.046 nsec
d) 0.0046 nsec
View Answer

Answer: c
Explanation: The delay unit of 1.2 micron technology is 0.046 nsec.

12. What is the transition point of an inverter?
a) Vdd
b) 0.5 Vdd
c) 0.25 Vdd
d) 2 Vdd
View Answer

Answer: b
Explanation: The transition point of an inverter is 0.5 Vdd. Transition point is the point where different phases of same substance can be obtained in equilibrium.

13. What is the desired or safe delay value for 5 micron technology?
a) 0.3 nsec
b) 0.5 nsec
c) 0.1 nsec
d) 0.2 nsec
View Answer

Answer: a
Explanation: The desired or safe delay value for 5 micron technology is 0.3 nsec.

1. Ids depends on
a) Vg

b) Vds
c) Vdd
d) Vss
View Answer

Answer: b
Explanation: Ids depends on both Vgs and Vds. The charge induced is dependent on gate to source voltage Vgs also charge can be moved from source to drain under influence of electric field created by Vds.

2. Ids can be given by
a) Qc x Ƭ
b) Qc / Ƭ
c) Ƭ / Qc
d) Qc / 2Ƭ
View Answer

Answer: b
Explanation: Ids can be given as charge induced in the channel(Qc) divided by transit time (Ƭ). Ids is equivalent to (-Isd).

3. Transit time can be given by
a) L / v
b) v / L
c) v x L
d) v x d
View Answer

Answer: a
Explanation: Transit time (Ƭ) can be given by lenght of channel(L) by velocity(v). Transit time is the time required for an electron to travel between two electrodes.

4. Velocity can be given as
a) μ / Vds
b) μ / Eds
c) μ x Eds
d) Eds / μ
View Answer

Answer: b
Explanation: Velocity can be given as the product of electron or hole mobility(μ) and electric field(Eds). It gives the flow velocity which an electron attains due to electric field.

5. Eds is given by
a) Vds / L
b) L / Vds

c) Vds x L
d) Vdd / L
View Answer

Answer: a
Explanation: Electric field(Eds) can be given as the ratio of Vds and L. Eds is the electric field created from drain to source due to volta Vds.

6. Mobility of proton or hole at room temperature is
a) 650 cm2/V sec
b) 260 cm2/V sec
c) 240 cm2/V sec
d) 500 cm2/V sec
View Answer

Answer: c
Explanation: The value of mobility of proton or hole at room temperature is 240 cm2/V sec. This gives the measure of how fast an electron can move.

7. In resistive region
a) Vds greater than (Vgs – Vt)
b) Vds lesser than (Vgs – Vt)
c) Vgs greater than (Vds – Vt)
d) Vgs lesser than (Vds – Vt)
View Answer

Answer: b
Explanation: In non saturated or resistive region, Vds lesser than Vgs – Vt where Vds is the voltage between drain and source, Vgs is the gate-source voltage and Vt is the threshold voltage.

8. The condition for saturation is
a) Vgs = Vds
b) Vds = Vgs – Vt
c) Vgs = Vds – Vt
d) Vds greater than Vgs – Vt
View Answer

Answer: b
Explanation: The condition for saturation is Vds = Vgs – Vt, since at this point IR drop in the channel equals the effective gate to channel voltage at the drain.

9. Threshold voltage is negative for
a) nMOS depletion
b) nMOS enhancement
c) pMOS depletion

d) pMOS enhancement
View Answer

Answer: a
Explanation: The threshold voltage for nMOS depletion denoted as Vtd is negative.

10. The current Ids _____ as Vds increases
a) increases
b) decreases
c) remains fairly constant
d) exponentially increases
View Answer

Answer: c
Explanation: The current Ids remains fairly constant as Vds increases in the saturation region.

11. In linear region, _____ channel exists
a) uniform
b) non-uniform
c) wide
d) uniform and wide
View Answer

Answer: a
Explanation: In linear region of MOSFET, the channel is uniform and narrow. This is the concentration distribution.

12. When the channel pinches off?
a) Vgs>Vds
b) Vds>Vgs
c) Vds>(Vgs-Vth)
d) Vgs>(Vds-Vth)
View Answer

Answer: c
Explanation: In MOSFET, in saturation region, when Vds > (Vgs – Vth), the channel pinches off that is the channel current at the drain spreads out.

13. When threshold voltage is more, leakage current will be
a) more
b) less
c) all of the mentioned
d) none of the mentioned
View Answer

Answer: b
Explanation: Increasing the threshold voltage, leads to small leakage current when turned off and reduces current flow when turned on.

14. MOSFET is used as
a) current source
b) voltage source
c) buffer
d) divider
View Answer

Answer: a
Explanation: MOSFET is used as current source. Bipolar junction transistor also acts as good current source.