EC8095 **VLSI DESIGN** **L T P C**
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OBJECTIVES:

- Study the fundamentals of CMOS circuits and its characteristics.
- Learn the design and realization of combinational & sequential digital circuits.
- Architectural choices and performance tradeoffs involved in designing and realizing the circuits in CMOS technology are discussed
- Learn the different FPGA architectures and testability of VLSI circuits.

UNIT I INTRODUCTION TO MOS TRANSISTOR 9

MOS Transistor, CMOS logic, Inverter, Pass Transistor, Transmission gate, Layout Design Rules, Gate Layouts, Stick Diagrams, Long-Channel I-V Charters tics, C-V Charters tics, Non ideal I-V Effects, DC Transfer characteristics, RC Delay Model, Elmore Delay, Linear Delay Model, Logical effort, Parasitic Delay, Delay in Logic Gate, Scaling.

UNIT II COMBINATIONAL MOS LOGIC CIRCUITS 9

Circuit Families: Static CMOS, Ratioed Circuits, Cascode Voltage Switch Logic, Dynamic Circuits, Pass Transistor Logic, Transmission Gates, Domino, Dual Rail Domino, CPL, DCVSPG, DPL, Circuit Pitfalls.
Power: Dynamic Power, Static Power, Low Power Architecture.

UNIT III SEQUENTIAL CIRCUIT DESIGN 9

Static latches and Registers, Dynamic latches and Registers, Pulse Registers, Sense Amplifier Based Register, Pipelining, Schmitt Trigger, Monostable Sequential Circuits, Astable Sequential Circuits.
Timing Issues : Timing Classification Of Digital System, Synchronous Design.

UNIT IV DESIGN OF ARITHMETIC BUILDING BLOCKS AND SUBSYSTEM 9

Arithmetic Building Blocks: Data Paths, Adders, Multipliers, Shifters, ALUs, power and speed tradeoffs, Case Study: Design as a tradeoff.

Designing Memory and Array structures: Memory Architectures and Building Blocks, Memor Core, Memory Peripheral Circuitry.

UNIT V IMPLEMENTATION STRATEGIES AND TESTING 9

FPGA Building Block Architectures, FPGA Interconnect Routing Procedures. Design for Testability: *Ad Hoc* Testing, Scan Design, BIST, IDDQ Testing, Design for Manufacturability, Boundary Scan.

TEXT BOOKS:

1. Neil H.E. Weste, David Money Harris -CMOS VLSI Design: A Circuits and Systems Perspective‖, 4th Edition, Pearson , 2017 (UNIT I,II,V)
2. Jan M. Rabaey ,Anantha Chandrakasan, Borivoje. Nikolic, ‖Digital Integrated Circuits:A Design perspective‖, Second Edition , Pearson , 2016.(UNIT III,IV)

REFERENCES

1. M.J. Smith, -Application Specific Integrated Circuits‖, Addisson Wesley, 1997
2. Sung-Mo kang, Yusuf leblebici, Chulwoo Kim -CMOS Digital Integrated Circuits:Analysis & Design‖,4th edition McGraw Hill Education,2013
3. Wayne Wolf, -Modern VLSI Design: System On Chip‖, Pearson Education, 2007
4. R.Jacob Baker, Harry W.LI., David E.Boyee, -CMOS Circuit Design, Layout and Simulation‖, Prentice Hall of India 2005.

UNIT I INTRODUCTION TO MOS TRANSISTOR
PART – A

1. **What is meant by VLSI?**
   Very large scale integration is the process of creating an integrated circuit by combining thousands of transistors in to a single chip.

2. **Define Threshold voltage for the MOSFET.**
   The Threshold voltage, V for a MOS transistor can be defined as the voltage applied V_T between the gate and the source of the MOS transistor below which the drain to source current, I_{DS} effectively drops to zero.

3. **What are the objectives of layout rules?**
   The objective associated with layout rules is to obtain a circuit with optimum yield (functional circuits versus non-functional circuits) in as small as area possible without compromising reliability of the circuit.

4. **Why NMOS transistor is selected as pull down transistor?**
   NMOS transistors produce "strong zeros," and PMOS devices generate "strong ones". An NMOS device pulls the output all the way down to GND, while a PMOS lowers the output no further than |VTp|. The PMOS turns off at that point, and stops contributing discharge current. NMOS transistors are hence the preferred devices in the PDN.

5. **What is the need of demarcation line?**
   In CMOS a demarcation line is drawn to avoid touching of p-diff with n-diff. All pMOS must lie on one side of the line and all nMOS will have to be on the other side.

6. **What is meant Channel length modulation in NMOS transistors?**
   The current between drain and source terminals is constant and independent of the applied voltage over the terminals. This is not entirely correct. The effective length of the conductive channel is actually modulated by the applied V. Increasing in V causes the depletion region at the drain junction to grow, reducing the length of the effective channel.

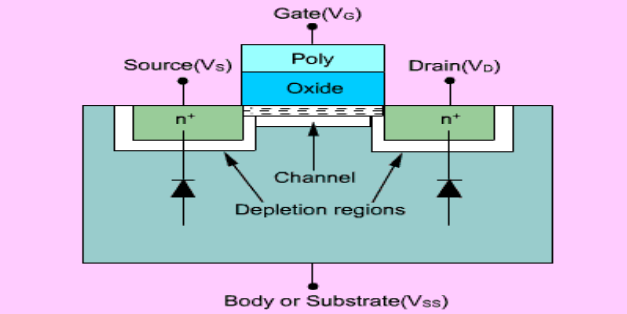
7. **What are the advantages of CMOS over NMOS?**
   a) Reduce complexity of the circuit b) low static power consumption
   c) high noise immunity d) high density of logic function on a chip

8. **Define propagation delay of a CMOS inverter.**
   The propagation delay of a CMOS inverter is the difference in time (calculated at 50% of input-output transition), when output switches, after application of input.

9. **Define Scaling.**
   Scaling is defined as the simplified guidelines for shrinking device dimensions to increase

transistor density & operating frequency and reduction in power dissipation & gate delays.

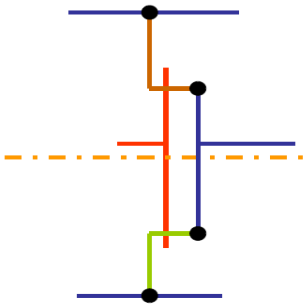
10. **Construct NMOS structure.**



11. **Define body bias effect.**

The threshold voltage V_T is not a constant with respect to the voltage difference between the body and the source of MOS transistor. This effect is called body-bias effect or body effect.

12. **Draw the Stick diagram for CMOS inverter.**



13. **State channel-length modulation. Write down the equation for describing the channel length modulation effect in NMOS transistors.**

The current between drain and source terminals is constant and independent of the applied voltage over the terminals. This is not entirely correct. The effective length of the conductive channel is actually modulated by the applied V. Increasing in V causes the depletion region at the drain junction to grow, reducing the length of the effective channel. The equation for describing the channel length modulation effect in NMOS transistor

$$I_D = I_D'(1 + \lambda V_{DS})$$

14. **List the various color coding used in stick diagram?**

a)n-diffusion Green b)p-diffusion yellow c) polysilicon red d) metal-1 blue

e) metal-2 dark blue or purple f) contact cut black g) via black

h) demarcation line brown i) Vdd orVss contact black

15. **What is Latch-up? How to prevent latch up?**

Latch up is a condition in which the parasitic components give rise to the establishment of low resistance conducting paths between V_{dd} and V_{ss} with disastrous results. Careful control during fabrication is necessary to avoid this problem.

16. **What is meant by pass transistor and transmission gate?**

When an nMos or pMOS is used alone as an imperfect switch, we call it as a **pass transistor.**

A circuit which passes both 0s and 1s in an acceptable fashion is called as **transmission gate or pass gate.**

17. **Explain noise margin.**

Noise margin is closely related to DC voltage characteristics. It allows to determine the allowable noise voltage on the input of a gate so that the output will not be corrupted. Two important parameters are used.

Low noise margin(NM_L): It is defined as the difference in maximum LOW input voltage recognized by receiving gate and the maximum LOW output voltage produced by the driving gate. $\mathbf{NM_L=V_{IL}-V_O}$.

Low noise margin(NM_H): It is defined as the difference in minimum HIGH output voltage of the driving gate and the minimum HIGH input voltage recognized by the receiving gate. $\mathbf{NM_H=V_{OH}-V_{IH}}$.

18. **Write short notes on Elmore delay model.**

The elmore delay model estimates the delay from a source switching to one of the leaf nodes changing as the sum over each node I of the capacitance C_i on the node, multiplied by the effective resistance R_{is} on the shared path from the source to the node and the leaf.

$$\mathbf{t_{pd} = \Sigma\, R_{is}\, C_i}$$

19. **Define logical effort.**

Logical effort of a gate is defined as the ratio of the input capacitance of the gate to the input capacitance of an inverter that can deliver the same output current.

20. **Define parasitic delay.**

The parasitic delay of a gate is the delay of the gate when it drives to zero load. A common method of computing parasitic delay is to count only diffusion capacitance on the output node.

PART-B & C

1. **Develop the layout design rules and draw diagram for four input NAND and NOR gate.**

Ref: “VLSI DESIGN ” by Jose Anand [Page.no:86-89]

2. **Explain the DC and transfer characteristics of a CMOS inverter with necessary conditions for the different regions of operation.**
   Ref: “VLSI DESIGN ” by Jose Anand [Page.no:55-59]
3. **Discuss the scaling principles and its limits.**
   Ref: “VLSI DESIGN ” by Jose Anand [Page.no:71-75]
4. **Discuss the mathematical equations that can be used to model the drain current and diffusion capacitance of MOS transistors.**
   Ref: “VLSI DESIGN ” by Jose Anand [Page.no:37-40]
5. **Explain the different steps involved in n-well CMOS fabrication process with neat diagram**
   Ref: “Jan Rabaey, Anantha Chandrakasan, B.Nikolic, “Digital Integrated Circuits [Page.no:76-78]
6. **Discuss in detail with a neat layout, the design rules for a CMOS inverter.**
   Ref: “VLSI DESIGN ” by Jose Anand [Page.no:86-89]
7. **Explain the DC transfer characteristics of a CMOS Inverter with necessary conditions for the different regions of operation.**
   Ref: “VLSI DESIGN ” by Jose Anand [Page.no:55-59]
8. **Explain the need of scaling, scaling principles and fundamental units of CMOS inverter.**
   Ref: “VLSI DESIGN ” by Jose Anand [Page.no:71-75]
9. **Discuss and model the equation for source to drain current in the three regions of operation of a MOS transistor and draw the VI characteristics.**
   Ref: “VLSI DESIGN ” by Jose Anand [Page.no:37-40]
10. **Construct the stick and layout diagram for NAND and NOR gate.**
    Ref: “VLSI DESIGN ” by Jose Anand [Page.no:86-89]
11. **Explain in detail about the body effect and its effect in MOS device.**
    Ref: “VLSI DESIGN ” by Jose Anand [Page.no:49-50]
12. **Analyse and Derive the noise margins for a CMOS inverter.**
    Ref: “VLSI DESIGN ” by Jose Anand [Page.no:60-61]

UNIT II COMBINATIONAL MOS LOGIC CIRCUITS
PART-A

1. **State the advantages of transmission gates.**

   The transmission gate passes over the entire voltage range. The transition resistance of the transmission gate varies depending upon the voltage to be switched, and corresponds to a superposition the resistance curves of the two transistors.

2. Define static CMOS.

In static CMOS, at every point in time (except during the switching transients), each gate output is connected to either V_{DD} or V_{SS} via a low resistance path. The output of the gate depends on the Boolean function implemented by the circuit.

3. Define Elmore constant

Elmore constant is used in the approximation of the delay through an RC network in an electronic system. It is often used in applications such as logic synthesis, delay calculation, static timing analysis, placement and routing, since it is simple to compute and is reasonably accurate.

4. Why single phase dynamic logic structure cannot be cascaded? Justify

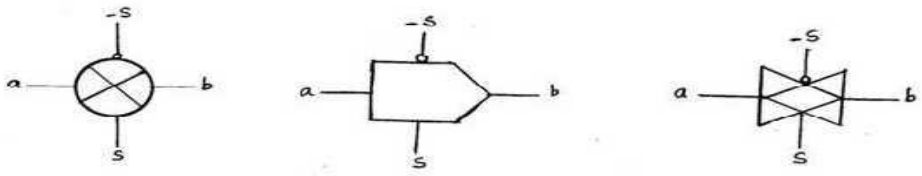
If several stages of the previous CMOS dynamic logic circuit are cascaded together using the same clock φ, a problem in evaluation involving a built-in "race condition" will exist

5. What is pass transistor logic?

Pass transistor logic (PTL) describes several logic families used in the design of integrated circuits. reduces the count of transistors used to make different logic gates, by eliminating redundant transistors. Transistors are used as switches to pass logic levels between nodes of a circuit, instead of switches connected directly to supply voltages. This reduces the number of active devices, but has the disadvantage that the difference of the voltage between high and low logic levels decreases at each stage.

6. What is Transmission gate and draw its symbols?

A transmission gate is similar to a relay that can conduct in both directions or block by a control sign with almost any voltage potential. It is a CMOS based switch in which PMOS passes a strong 1 but poor and NMOS passes strong 0 but poor 1. Both PMOS and NMOS work simultaneously.



7. Compare and contrast synchronous design and asynchronous design.

Synchronous circuits change state with every clock signal, with the state changing according to what the inputs are. Asynchronous circuits change states whenever the inputs change.

8. What is bubble pushing ?

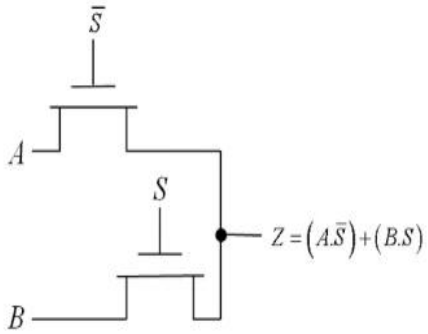
- Bubble pushing is a technique to apply De Morgan's theorem directly to the

logic diagram.

- Change the logic gate (AND to OR and OR to AND).
- Add bubbles to the inputs and outputs where there were none, and remove the original bubbles.

➢ Logic gates can be De Morganized so that bubbles appear on inputs or outputs in order to satis signal conditions rather than specific logic functions. An active- low signal should be connected to a bubble on the input of a logic gate.

9. Draw 2:1 Multiplexer using pass transistor logic.



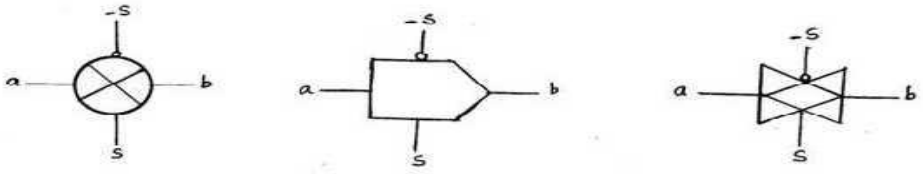
10. What are the sources of static power dissipation ?

Leakage current or other current drawn continuously from the power supply are the sources of static power dissipation

11. What is Transmission gate and draw its symbols?

A transmission gate is similar to a relay that can conduct in both directions or block by a control signal with almost any voltage potential. It is a CMOS based switch in which PMOS passes a strong 1 but poor 0 and NMOS passes strong 0 but poor 1.

Both PMOS and NMOS work simultaneously.



12. List the types of power dissipation. (N/D-2017)

(i) Static power dissipation

(ii) Dynamic power dissipation

(iii) Short circuit power dissipation

13. Define body bias effect. (N/D-2016)

The threshold voltage V_T is not a constant with respect to the voltage difference between the body and the source of MOS transistor. This effect is called body-bias effect or body effect.

14. List out the sources of static and dynamic power consumption. (N/D-2016)

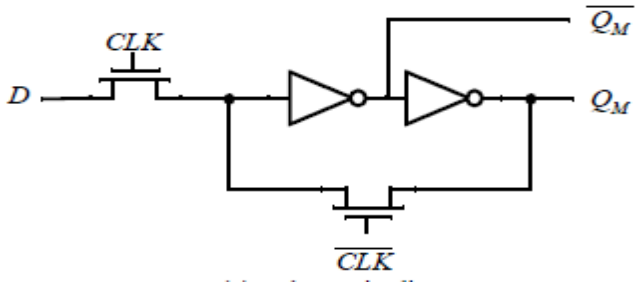
i) Static dissipation due to

-leakage current or other current drawn continuously from the power supply

ii) Dynamic dissipation due to

- Switching transient current
- Charging and discharging of load capacitances.

15. Draw the switch level schematic of multiplexer based nMOS latch using nMos only pass transistors for multiplexer



16. What are the major circuit pitfalls?

- Threshold drops
- Ratio failures
- Leakage
- Charge sharing
- Power supply noise
- Coupling
- Minority carrier injection

17. What is static power?

Static power is power consumed even when a chip is not switching.

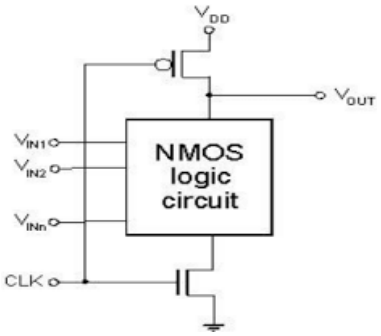
18. Define ratioed logic.

Ratioed logic is an alternative method to reduce the number of transistors required to implement a given logic function at the cost of reduced robustness and an extra power dissipation.

In ratioed logic, a gate consists of a nMOS pull down network in order to implement the logic function and the entire pull up network in order to implement the logic function and the entire pull up network is replaced with a single unconditional load device that pulls up the output for a HIGH value when PDN is OFF.

19. What is domino logic and draw its structure?

Domino logic is a CMOS-based evolution of the dynamic logic techniques based on either PMOS or NMOS transistors. It allows a rail-to-rail logic swing. It was developed to speed up circuits.



20. What is dynamic power dissipation?

Power dissipation is due to circuit switching to charge and discharge the output load capacitance at a particular node at operating frequency is called dynamic power dissipation. It is due to,Charging and discharging of load capacitances as gate switches Short circuit current when both pMOS and nMOS are partially ON.

PART-B & C

1. **Explain the dynamic power dissipation in CMOS circuits with necessary diagrams and expressions.**

   Ref: "VLSI DESIGN " by Jose Anand [Page.no:151]

2. **Write short notes on**

   - **Ratioed Circuits**
   - **Dynamic CMOS Circuits**

   Ref: "VLSI DESIGN " by Jose Anand [Page.no:126-131,137-141]

3. **Discuss in detail various static latches and registers.**

   Ref: "VLSI DESIGN " by Jose Anand [Page.no:156-165]

4. **Discuss about the design of sequential dynamic circuits and its pipelining concept.**

   Ref: "VLSI DESIGN " by Jose Anand [Page.no:178-183]

5. **Explain the operation of master-slave based edge triggered register.**

Ref: "VLSI DESIGN " by Jose Anand [Page.no:159-163]

6. **Draw the CMOS logic circuit for the Boolean expression**

Z = [A(B + C) + DE] and explain.

Ref: "VLSI DESIGN " by Jose Anand [Page.no:109-112]

7. **Discuss the low power design principles in detail.**

Ref: "VLSI DESIGN " by Jose Anand [Page.no:152-153]

8. **Explain about DCVSL logic with suitable example.**

Ref: "VLSI DESIGN " by Jose Anand [Page.no:129-130]

9. **Write short notes on :**

- **True single-phase clocked register**
- **NORA – CMOS latches.**

Ref: "VLSI DESIGN " by Jose Anand [Page.no:168-169,180-183]

10. **Explain static and dynamic latches and registers in detail**

Ref: "VLSI DESIGN " by Jose Anand [Page.no:155-168]

11. **Discuss in detail the characteristics of CMOS transmission gate?**

Ref: "VLSI DESIGN " by Jose Anand [Page.no:107-108]

UNIT – III

SEQUENTIAL CIRCUIT DESIGN

1. **What is meant by pipelining? (A/M-2017)**

Pipelining is a popular design technique often used to accelerate the operation of the data paths in digital processors. The major advantages of pipelining are to reduce glitching in complex logic networks and getting lower-energy due to operand isolation.

2. **Compare and contrast synchronous design and asynchronous design. (A/M-2017)**

Synchronous circuits change state with every clock signal, with the state changing according to what the inputs are. Asynchronous circuits change states whenever the inputs change.

3. **What is NORA CMOS ? (N/D-2017)**

NORA means NO RAce

During φ low (φ' high), each stage pre-charges

– N logic stages pre-charge to Vdd; P logic stages pre-charge to GND

When φ goes high (φ' low), each stage enters the evaluation phase

– N logic evaluates to GND; P logic stages evaluate to Vdd

– All NMOS and PMOS stages evaluate one after another in succession, as in Domino logic

4. Define clock jitter. (N/D-2017)

Clock jitter is defined as the Temporal variations in consecutive edges of the clock signals; modulation + random noise-Cycle-to-cycle(short-term) long term.

5. Define Clock Skew.

Clock skew is defined as spatial variation in temporally equivalent clock edges.

6. Define Set up and Hold time.

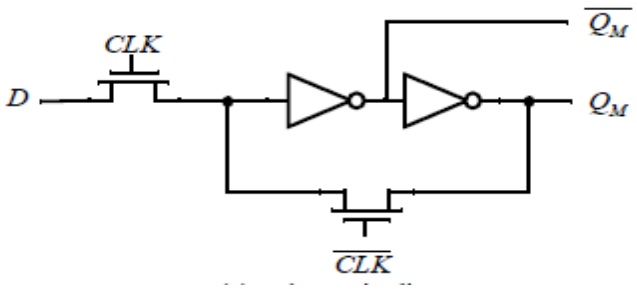
Setup time: The amount of time before the clock edge that data input D must be stable the rising clock edge arrives.

Hold time: This indicates the amount of time after the clock edge arrives that data input D must be held stable in order for the flip-flop to latch the correct value.

7. What is bi stability?

Static memories use positive feedback to create a bistable circuit — a circuit having two stable states that represent 0 and 1.

8. Draw the switch level schematic of multiplexer based nMOS latch using nMos only pass transistors for multiplexer (A/M-2016)



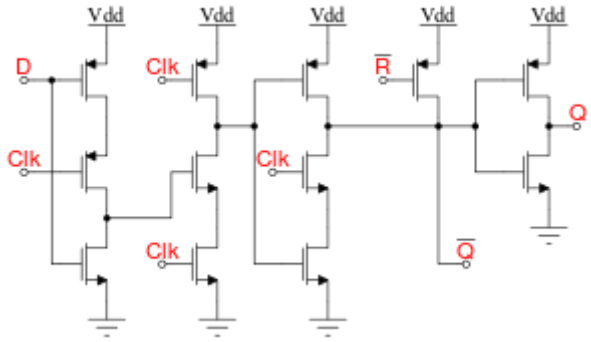
9. What is clocked CMOS register (A/M-2016)

In integrated circuit design, dynamic logic (or sometimes clocked logic) is a design methodology in combinatory logic circuits, particularly those implemented in MOS technology. It is distinguished from the so-called static logic by exploiting temporary storage of information in stray and gate capacitances.

10. What is meant by pipelining? (N/D-2016)

Pipelining is a popular design technique often used to accelerate the operation of the data paths in digital processors. The major advantages of pipelining are to reduce glitching in complex logic networks and getting lower-energy due to operand isolation.

11. Draw the schematic of dynamic edge-triggered register. (N/D-2016)



12. Define Propagation delay and Contamination delay.

Propagation delay(tpd):The amount of time needed for a change in a logic input to result in a permanent change at an output, that is the combinational logic will not show any further output changes in response to an input change alter time fod units.

Contamination delay(tea): The amount of time needed for a change in a logic input to result in an initial change at an output, that is the combinational logic is guaranteed not to show any output change in response to an input change before fed time units have passed.

13. Compare Latches and Registers.

- Latch stores data when clock is low
- Register stores data when clock rises

14. What are positive and negative latches?

- Negative latch is transparent when CLK= 0
- Positive latch is transparent when CLK= 1

15. Define pulse register?

It used the *master-slave* configuration to create an constructing a register uses pulse signals. The *edge-triggered* register. A fundamentally different approach for idea is to construct a short pulse around the rising (or falling) edge of the clock. This pulse acts as the clock input to a latch, sampling the input only in a short window. Race conditions are thus avoided by keeping the opening time (i.e, the *transparent* period) of the latch very short. The combination of the glitchgeneration circuitry and the

latch results in a *positiveedge-triggered* register.

16. What is Sense-Amplifier Based Registers

The technique that uses a *sense amplifier* structure to implement an *edge-triggered* register .*Sense amplifier* circuits accept small input signals and amplify them to generate rail-to-rail swings. As we will see, *sense amplifier* circuits are used extensively in memory cores and in low swing bus drivers to amplify small voltage swings present in heavily loaded wires.

17. Define Schmitt Trigger

A Schmitt trigger is a device with two important properties:

1. It responds to a slowly changing input waveform with a *fast transition time at the output*.

2. The voltage-transfer characteristic of the device displays *different switching thresholds for positive- and negative-going input signals*, a typical voltage-transfer characteristic of the Schmitt trigger is shown(and its schematics symbol). The switching thresholds for the low-to-high and highto-low transitions are called *VM+* and *VM-*, respectively.

18. What is monosatble sequential circuits?

A monostable element is a circuit that generates *a pulse of a predetermined width* every time the quiescent circuit is triggered by a pulse or transition event. It is called *monostable* because it has only one stable state (the quiescent one). A trigger event, which is either a signal transition or a pulse, causes the circuit to go temporarily into another quasi-stable state. This means that it eventually returns to its original state after a time period determined by the circuit parameters. This circuit, also called a *one-shot*, is useful in generating pulses of a known length.

19. Write the Classification of Digital Systems.

- Synchronous Interconnect
- Mesochronous interconnect
- Plesiochronous Interconnect
- Asynchronous Interconnect

20. what is monosatble sequential circuits?

An astable circuit has no stable states. The output oscillates back and forth between two quasi-stable states with a period determined by the circuit topology and parameters (delay,power supply, etc.). One of the main applications of oscillators is the on-chip generation of clock signals.

PART-B & C

1. **Discuss in detail various static latches and registers. (N/D-2016)**

   Ref: "VLSI DESIGN " by Jose Anand [Page.no:156-165]

2. **Explain the timing basics and clock distribution techniques in synchronous design in detail. (N/D-2017)**

   Ref: "VLSI DESIGN " by Jose Anand [Page.no:172-176]

3. **Discuss about the design of sequential dynamic circuits and its pipelining concept. (N/D-2017)**

   Ref: "VLSI DESIGN " by Jose Anand [Page.no:178-183]

4. **Explain different type of memory architecture and control unit in detail.**

   Ref: "VLSI DESIGN " by Jose Anand [Page.no:190-206]

5. **Explain the operation of True Single Phase Clocked Register (A/M-2017)**

   Ref: "VLSI DESIGN " by Jose Anand [Page.no:168-169]

6. **Draw and explain the operation of Conventional, pulsed and resettable latches.(A/M-2017)**

   Ref: "VLSI DESIGN " by Jose Anand [Page.no:155-64]

7. **Write short notes on :**

   - **True single-phase clocked register (N/D-2016)**
   - **NORA – CMOS latches. (N/D-2016)**

   Ref: "VLSI DESIGN " by Jose Anand [Page.no:168-169,180-183]

8. **Explain the operation of master-slave based edge triggered register. (M/J-2016)**

   Ref: "VLSI DESIGN " by Jose Anand [Page.no:159-163]

9. **Explain the concept of timing issues and pipelining. (A/M-2017)**

   Ref: "VLSI DESIGN " by Jose Anand [Page.no:169-182]

10. **Explain Classification of Digital Systems in detail**

    Ref: "Digital integrated circuits" by Jan m. Rabaey, Anantha chandrakasan, and Borivoje nikolic.[page no:43-46]

11. **State and explain monostable and bistable sequential circuits.**

    Ref: "Digital integrated circuits" by Jan m. Rabaey, anantha chandrakasan, and borivoje nikolic.[page no:309-311]

UNIT-IV

DESIGN OF ARITHMETIC BUILDING BLOCKS AND SUBSYSTEM

1. What is a datapath?

The datapath is the core of the processor that is all computations are performed. A typical datapath consists of an interconnection of basic combinational elements like shifters, adders, multipliers which can perform addition, multiplication, comparison, shifting and logical functions(AND, OR, XOR)

2. List out the components of data path? (A/M-2017)

A data path is a collection of functional units such as arithmetic logic units or multipliers, that perform data processing operations, registers, and buses. Along with the control unit it which composes, the central processing unit.

3. Give the application of high speed adder. (A/M-2017)

- The core of every microprocessor and digital signal processor is its data path. The heart of data-path and addressing units in turn are arithmetic units which include adders.
- Design of Arithmetic-Logic Units, floating-point arithmetic data paths, and in address generation units. Moreover, digital signal processing makes extensive use of high speed addition in the implementation of digital filters.

4. How to design a high speed adder? (N/D-2017)

First we should examine a realization of a one-bit adder which represents a basic building block for all the more elaborate addition schemes.

Operations of a Full Adder is defined by the Boolean equations for the sum and carry signals shown in this slide: ai, bi, and ci are the inputs to the i-th full adder stage, and si and ci+1 are the sum and carry outputs from the i-th stage, respectively.

5. What is latency? (N/D-2017)

Latency is a time interval between the stimulation and response, or, from a more general point of view, a time delay between the cause and the effect of some physical change in the system being observed.

6. What are shifters?

Shifters are used to shift the numbers from one bit position to other. Shifts can either be performed by a constant or variable amount. Constant shifts are trivial in hardware, requiring only wires. The

various types of shifters are as follows,

(i) Logical shifter

(ii) Arithmetic shifter.

(ii) Barrel shifter.

7. What are the advantages of barrel shifter?

- Signal has to pass through at most one transmission gate
- Propagation delay is constant and independent of the shift value
- Used for small shift values.

8. What is ALU and give its significance.

An arithmetic logic unit (ALU) is a combinational digital electronic circuit that performs arithmetic and bitwise operations on integer binary numbers. An ALU is a fundamental building block of many types of computing circuits, including the central processing unit (CPU) of computers, FPUs, and graphics processing units (GPUs). A single CPU, FPU or GPU may contain multiple ALUs. The inputs to an ALU are the data to be operated on, called operands, and a code indicating the operation to be performed; the ALU's output is the result of the performed operation. In many designs, the ALU also has status inputs or outputs, or both, which convey information about a previous operation or the current operation, respectively, between the ALU and external status registers.

9. Write any two design process of data path circuits

A datapath is a collection of functional units such as arithmetic logic units or multipliers, that perform data processing operations, registers, and buses. Along with the control unit it composes the central processing unit

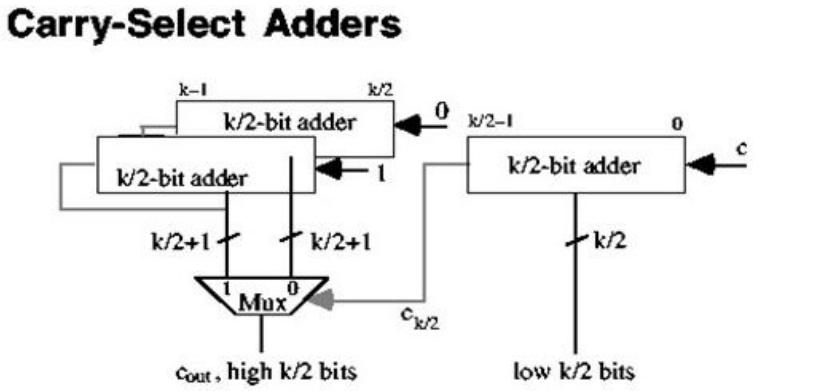
- A data path is best implemented in a **bit-sliced fashion**. A single layout is used repetitively for every bit in the data word. This regular approach eases the design effort and results in fast and dense layouts
- **Optimum sliced data path** circuits by rigorously optimizing transistor sizes and topologies.

10. What is meant by bit-sliced data path organization (A/M-2016)

Data path is the core of a processor. It is where all computations are performed. They are generally arranged in a bit sliced organization. Instead of operating on single bit digital signals , the data in a processor is arranged ina word based fashion. A 32 bit processor operates on data words that are 32 bit wide. Since the same operation has to be performed on each bit of the data word , the data path cosists of

32 identical slices, each of them operating on a single bit. So the name bit sliced. Data path designer can concentrate on the design of a single slice that is repeated 32 times.

11. Determine propagation delay of n-bit carry select adder. (A/M-2016)



Carry-select adder for k-bit numbers built from three k/2-bit adders.

$$C_{select\text{-}add}(k) = 3C_{add}(k/2) + k/2 + 1$$
$$T_{select\text{-}add}(k) = T_{add}(k/2) + 1$$

12. What is barrel shifter? (N/D-2016)

A barrel shifter is a digital circuit that can shift a data word by a specified number of bits without the use of any sequential logic, only pure combinatorial logic. One way to implement it is as a sequence of multiplexers where the output of one multiplexer is connected to the input of the next multiplexer in a way that depends on the shift distance.

A barrel shifter is often used to shift and rotate n-bits in modern microprocessors, typically within a single clock cycle. Thus barrel shifter very useful in the designing of arithmetic circuits.

13. Write the principle of any one fast multiplier? (N/D-2016)

- Partial product generation
- Partial product accumulation

14. List out the types of high speed adder.

- Ripple carry adder
- Carry look ahead adder
- Carry save adder

15. Give some applications of multipliers in digital circuits.

- Datapath in microprocessor

- MAC (multiply and accumulate) structures
- ALU(Arithmetic and logical unit)
- High speed integrated circuits
- Filter design, convolution in Digital signal processing applications

16. Comment on performance of Ripple carry Adder

It is linearly proportional to the no of bits. It reduces the delay of the carry path. It reduces the capacitance of carry bit

17. What is meant by accumulator?

In a computer's central processing unit (CPU), an accumulator is a register in which intermediate arithmetic and logic results are stored. It acts as a part of arithmetic and logic unit (ALU).

18. What are the different multipliers available?

- Array multiplier
- Booth multiplier
- Wallace tree multiplier

19. Write the steps in Wallace tree algorithm.

1. Multiply each bit of one of the arguments by each bit of the other yielding n^2 results.
2. Reduce the number of partyial products to two using layers of full and half adders.
3. Group the wires in two numbers and add them with a conventional adder

20. List the advantages and disadvantages of dual rail domino adder

Advantages

1. Very fast
2. Used in fast multipliers

Disadvantages

1. Occupies larger area.
2. More power consumption.

PART-B & C

1. Explain the operation of a basic 4 bit adder. Describe the different approaches of improving the speed of the adder. (N/D-2016)

Ref: "VLSI DESIGN " by Jose Anand [Page.no:216-218]

2. Design a 16 bit carry bypass and carry select adder and discuss their features.

(M/J-2016)

Ref: "VLSI DESIGN " by Jose Anand [Internet/PPT]

3. **Draw the structure of ripple carry adder and explain its operation. How the drawback in ripple carry adder overcome by carry look ahead adder and discuss. (N/D-2017)**

   Ref: "VLSI DESIGN " by Jose Anand [Page.no:216-218]

4. **Design a multiplier for 5 bit by 3 bit Explain its operation and summarize the number of adders Discuss it over Wallace multiplier.**

   (N/D-2017)

   Ref: "VLSI DESIGN " by Jose Anand [Page.no:229-231]

5. **Explain the concept of modified Booth multiplier with a suitable example. (A/M-2017)**

   Ref: "VLSI DESIGN " by Jose Anand [Page.no:224-226]

6. **Explain barrel shifter and its operation in detail.**

   Ref: "VLSI DESIGN " by Jose Anand [Page.no:236-238]

7. **Explain the operation of booth multiplication with suitable examples? Justify how booths algorithm speed up the multiplication process (N/D-2016)**

   Ref: "VLSI DESIGN " by Jose Anand [Page.no:224-226]

8. **Design a 4 x 4 array multiplier and write down the equation for delay. (M/J-2016)**

   Ref: "VLSI DESIGN " by Jose Anand [Page.no:227-228]

9. **Explain the concept of carry look ahead adder with neat diagram. (A/M-2017)**

   Ref: "VLSI DESIGN " by Jose Anand [Page.no:218-221]

10. **Discuss the details about speed and area trade off. (A/M-2017)**

    Ref: "VLSI DESIGN " by Jose Anand [Page.no:239-251]

11. **Explain ALU and give its importance in processor.**

    Ref: "VLSI DESIGN " by Jose Anand [Page.no:238-239]

12. **Explain the architectures of ripple carry adder.**

    Ref: "VLSI DESIGN " by Jose Anand [Page.no:216-218]

UNIT-V
IMPLEMENTATION STRATEGIES AND TESTING

1. **What is meant by CBIC? (A/M-2017)**

   A cell-based ASIC uses predesigned logic cells (e.g. AND gates, OR gates, multiplexers, and flip-plops,) known as standard cells, also pronounced as "Sea Bick" or CBIC. The CBIC are built of rows of standard cells like a wall built of bricks. The standard cell areas may be used in combination with microcontrollers or even microprocessors.

2. **Name the elements in a Configuration Logic Block (A/M-2017)**
    - Combinational logic
    - Flip flops
3. **What is ULSI? (N/D-2017)**

ULSI ie., Ultra large-scale integration (ULSI) is the process of integrating or embedding millions of transistors on a single silicon semiconductor microchip and also refers loosely to placing more than about one million circuit elements on a single chip. The Intel 486 and Pentium microprocessors, for example, use ULSI technology.

4. **Write the various ways of routing procedure (N/D-2017)**
    - Global routing
        - Line routing
        - Maze routing
    - Detailed routing
        - Channel routing
        - Switch box routing
5. **What is a primitive cell?**

Primitive cell is a unit cell that contains exactly one lattice point. It is the smallest possible cell. If there is a lattice point at the edge of a cell and thus shared with another cell, it is only counted half. Accordingly, a point located on the corner of a cube is shared by 8 cubes and would count with 1/8.

6. **List the advantages of CBIC.**
    - Less cost
    - Less time
    - Reduced risk
    - Standard cell is optimized individually
    - Transistor operate at maximum speed
7. **State the feature of full custom design.**

In a full custom ASIC, an engineer designs some or all of the logic cells, circuits or layout specifically for one ASIC. It makes sense to take this approach only if there are no suitable existing cell libraries available that can be used for the entire design.

8. **What arc feed through cells? State their uses. (A/M-2016)**

Feed though is a piece of metal used to pass a signal through cell or to a space. Feed through cells needed for vertical routing for routing using the same metal layer(s) as within cells

9. **State the features of full custom design. (A/M-2016)**

In a full custom ASIC, an engineer designs some or all of the logic cells, circuits or layout specifically for one ASIC. It makes sense to take this approach only if there are no suitable existing cell libraries available that can be used for the entire design.

10. **What is the standard cell based ASIC design? (N/D-2016)**

A cell-based ASIC uses predesigned logic cells (e.g. AND gates, OR gates, multiplexers, and flip-plops,) known as standard cells, also pronounced as "Sea Bick" or CBIC. The CBIC are built of rows of standard cells like a wall built of bricks. The standard cell areas may be used in combination with microcontrollers or even microprocessors.

11. **What is an antifuse? State its merits and demerits (N/D-2016)**

An antifuse is normally high resistance (>100M). On application of appropriate programming voltages, the antifuse is changed permanently to a low-resistance structure (200-500).

12. **What is an Interconnect?**

Interconnect is a element which interconnects the different elements in the IC. Interconnect involves in routing procedure particularly in loose routing and detailed routing in the design process of FPGA

13. **Define flexible blocks.**

The predesigned logic cells are known as standard cells. The standard cell areas are called flexible blocks. These flexible blocks can be adjusted and optimized based on the design procedure of FPGA.

14. **What is FPGA? Give its importance**

A field-programmable gate array (FPGA) is an integrated circuit designed to be configured by a customer or a designer after manufacturing – hence "field-programmable". The FPGA configuration is generally specified using a hardware description language (HDL), similar to that used for an application-specific integrated circuit (ASIC).

15. **State the types of Design for Testability(DFT)**

Design for Testability(DFT).

These may be categorized as follows:

- *Ad hoc* testing

- Scan-based approaches
- Built-in self-test (BIST)

16. Write the techniques for ad hoc testing

The common techniques for ad hoc testing:

- Partitioning large sequential circuits
- Adding test points
- Adding multiplexers
- Providing for easy state reset

17. State scan design testability.

The *scan-design* strategy for testing has evolved to provide observability and controllability at each register. In designs with scan, the registers operate in one of two modes. In *normal mode*, they behave as expected. In *scan mode*, they are connected to form a giant shift register called a *scan chain* spanning the whole chip. By applying *N* clock pulses in scan mode,all *N* bits of state in the system can be shifted out and new *N* bits of state can be shifted in.

18. State BIST.

Self-test and built-in test techniques, as their names suggest, rely on augmenting circuits to allow them to perform operations upon themselves that prove correct operation. These techniques add area to the chip for the test logic, but reduce the test time required and thus can lower the overall system cost. [Stroud02] offers extensive coverage of the subject from the implementer's perspective.

19. Define IDDQ test.

A method of testing for bridging faults is called IDDQ test (*V* supply current Quiescent) or supply current monitoring. This relies on the fact that when a CMOS logic gate is not switching, it draws no DC current (except for leakage). When a bridging fault occurs, then for some combination of input conditions, a measurable DC *IDD* will flow. Testing consists of applying the normal vectors, allowing the signals to settle, and then measuring *IDD*. As potentially only one gate is affected, the IDDQ test has to be very sensitive

20. What is Boundary scan?

The increasing complexity of boards and the movement to technologies such as surface mount technologies (with an absence of through board vias) resulted in system design-ers

agreeing on a unified scan-based methodology called *boundary scan* for testing chips at the board (and system)

level. Boundary scan was originally developed by the Joint Test Access Group and hence is commonly referred to as JTAG. Boundary scan has become a popular standard interface for controlling BIST features as well.

PART-B

1. **With neat sketch explain the CLB,IOB and programmable interconnects of an FPGA device. (M/J-2016)**
   Ref: "VLSI DESIGN " by Jose Anand [Page.no:262]
2. **Write short notes on**
   Full custom ASIC (M/J-2016)
   Semi-custom ASIC (M/J-2016)
   Ref: "VLSI DESIGN " by Jose Anand [Page.no:254-260]
3. **Draw and explain the building blocks of FPGA. (N/D-2017)**
   Ref: "VLSI DESIGN " by Jose Anand [Page.no:266]
4. **Write short note on routing procedures involved in FPGA interconnect. (A/M-2017)**
   Ref: "VLSI DESIGN " by Jose Anand [Page.no:216-218]
5. **Explain different types of XILINX (3000,4000) architecture in details (A/M-2017)**
   Ref: "VLSI DESIGN " by Jose Anand [Page.no:270-272]
6. **Explain different types testability in detail.**
   Ref: "CMOS VLSI DESIGN " by Neil H. E. Weste & David Money Harris[Page.no:681]
7. **Explain Design for Manufacturability in detail**
   Ref: "CMOS VLSI DESIGN " by Neil H. E. Weste & David Money Harris[Page.no:687]
8. **Explain IDDQ testability in detail**
   Ref: "CMOS VLSI DESIGN " by Neil H. E. Weste & David Money Harris[Page.no:687]
9. **Explain *the techniques involved in Ad Hoc* Testing**
   Ref: "CMOS VLSI DESIGN " by Neil H. E. Weste & David Money Harris[Page.no:681]
10. **Explain *the techniques scan design* Testing in detail.**
    Ref: "CMOS VLSI DESIGN " by Neil H. E. Weste & David Money Harris[Page.no:682]

Reg. No. : | | | | | | | | | | | | |

Question Paper Code : 20421

B.E./B.Tech. DEGREE EXAMINATION, NOVEMBER/DECEMBER 2018.

Sixth/Seventh/Eighth Semester

Electronics and Communication Engineering

EC 6601 — VLSI DESIGN

(Common to Electrical and Electronics Engineering, Biomedical Engineering, Electronics and Instrumentation Engineering, Medical Electronics, Robotics and Automation engineering)

(Regulations 2013)

(Also Common to PTEC 6601 — VLSI Design for B.E. (Part-Time) Fifth Semester – Electronics and Communication Engineering and Third Semester – Electrical and Electronics Engineering – Regulation 2014)

Time : Three hours Maximum : 100 marks

Answer ALL questions.

PART A — (10 × 2 = 20 marks)

1. Why NMOS device conducts strong zero and weak one?

2. Draw the stick diagram of static CMOS 2-input NAND gate.

3. Determine the discharging time of the circuit shown in Figure-1. when switch 'A' is closed.

   Assume C_L and internal capacitances C_1 and C_2 are charged initially. Let

   $C_L = C_1 = C_2 = C$.

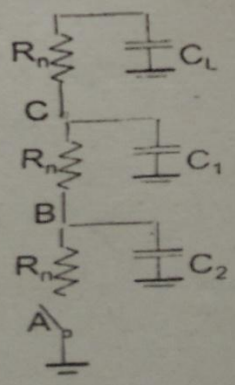


Fig 1

4. Realize X = B+ C and $Y = (A.(B + C))$ using multiple output domino stages.

5. List out the advantages and limitations of 3 T DRAM over 1 T DRAM.

6. List out the advantage of C^2MOS logic based register over pass-transistor logic based master-slave register.

7. The circuit in Fig.2 shows a carry propagation path in an adder circuit. Let A,B.C_i are the inputs to adder circuit and φ is the clock signal. Write the logic expressions for the signal *X*, *Y* to generate output carry.

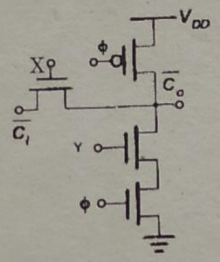


Fig. 2

8. Draw a 4-bit ripple carry adder and find its critical path delay.

9. Compare between Xilinx CLB interconnect and Alter a LAB interconnect.

10. Differentiate between full custom design and semi custom design.

PART B — (5 × 13 = 65 marks)

11. (a) (i) List out the goals of CMOS technology scaling. Explain How common electric field scaling is superior than constant voltage scaling. (7)

(ii) Derive the expression to obtain the minimum delay through the chain of CMOS inverter. (6)

Or

(b) (i) Explain the design techniques that are used for larger fan-in devices to reduce delay. (8)

(ii) Draw the small signal model of device during cut-off, linear and saturation region. (5)

12. (a) (i) Implement the equation $X = \overline{(A + B)CD}$ using complementary CMOS logic.

(1) Size the devices so that the output resistance is the same as that of an inverter with an NMOS W/L = 4 and PMOS W/L = 8.

(2) What are the input patterns that give the worst case t_{PHL} and t_{PLH}. Consider the effect of the capacitances at the internal nodes.

(3) If $P(A=1)=0.5$, $P(B=1)=0.2$, $P(C=1)=0.3$, $P(D=1)=1$, determine the power dissipation in the logic gate. Assume $V_{DD}=2.5V$, $C_{out}=30\,fF$ and $F_{clk}=250$ MHz. (7)

(ii) List out the limitations of pass transistor logic. Explain any two techniques used to overcome the drawback of pass transistor logic design. (6)

Or

(b) (i) Explain in detail the signal integrity issues in dynamic logic design. propose any two solutions to overcome it. (7)

(ii) (1) Determine the truth table for the circuit shown Figure-3. What logic function does it implement? (4)

(2) If the PMOS were removed, would the circuit still function correctly? Does the PMOS transistor serve any useful purpose? (2)

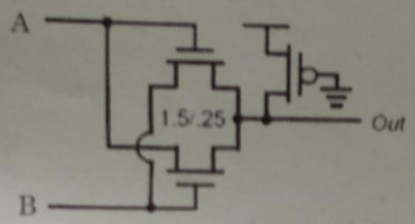


Fig 3

13. (a) (i) Identify the type of register for the circuit shown in figure 4 and express set up time, hold time and propagation delay of register in terms of the propagation delay of inverters and transmission gates. (5)

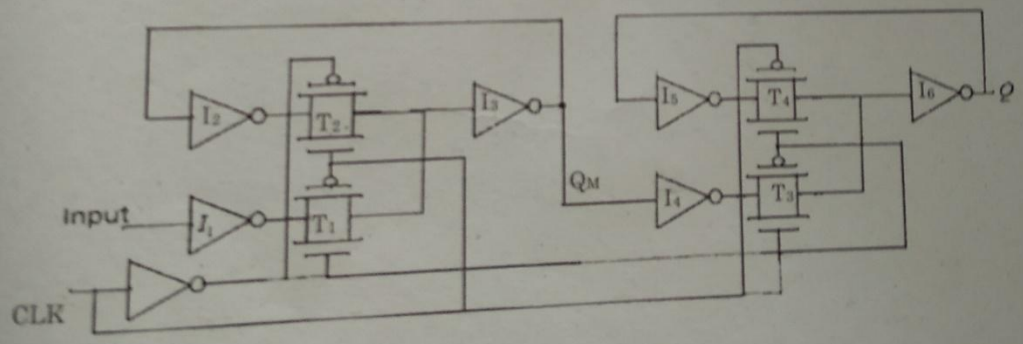


Fig. 4

(ii) Implement the register of question 13(i) using C²MOS logic and explain how 0-0 and 1-1 overlap of clock signals are eliminated. (8)

Or

(b) (i) Construct 6T based SRAM cell. Explain its read and write operations. What is the importance of Cell ratio and Pull up ratio in 6T SRAM cell? (8)

(ii) Analyze the impact of spatial variations of clock signal on edge-triggered sequential logic circuits. (5)

14. (a) Design an 8-bit Brent-Kung Adder. (13)

Or

(b) (i) Construct 4 × 4 Array type multiplier and find its critical path delay. (8)

(ii) Design 4-input and 4-output barrel shift adder using NMOS logic. (5)

15. (a) Explain CLB of Xilinx 4000 architecture. (13)

Or

(b) (i) Realize the function, $F = A.B + (B'C) + D$ using ACTEL (ACT-1) FPGA. (5)

(ii) Draw the flow chart of digital circuit design techniques. (4)

(iii) Differentiate between Hard Macro and Soft Macro. (4)

PART C — (1 × 15 = 15 marks)

16. (a) Derive an expression to show the drain current of MOS for various operating region. Explain one non-ideality for each operating region that changes the drain current. (15)

Or

(b) Explain in detail the CMOS manufacturing process. (15)

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97

Question Paper Code : 40965

B.E./B.Tech. DEGREE EXAMINATION, APRIL/MAY 2018
Sixth/Seventh/Eighth Semester
Electronics and Communication Engineering
EC 6601 – VLSI DESIGN
(Common to Biomedical Engineering/Electrical and Electronics Engineering/ Electronics and Instrumentation Engineering/Medical Electronics/Robotics and Automation Engineering)
(Regulations 2013)

Time : Three Hours | Maximum : 100 Marks

Answer ALL questions

PART – A **(10×2=20 Marks)**

1. What is velocity saturation effect ?
2. List the scaling principles.
3. Define Elmore's constant.
4. List the types of power dissipation.
5. Define clock skew.
6. Compare Registers and Latches.
7. Write the full adder output interms of propagate and generate.
8. Draw the structure of 4 × 4 barrel shifter.
9. What is the role of cell libraries in ASIC design ?
10. What are the two different types of routing ?

PART – B **(5×13=65 Marks)**

11. a) Explain the dynamic behavior of MOSFET transistor with neat diagram. **(6+7)**

(OR)

b) Write the layout design rules and draw diagram for four input NAND and NOR gate. **(6+7)**

12. a) i) Draw the CMOS logic circuit for the Boolean expression $Z = [A(B + C) + DE]'$ and explain. (6)

ii) Explain the basic principle of transmission gate in CMOS design. (7)

(OR)

b) Briefly discuss the signal integrity issues in dynamic design. (13)

13. a) Discuss about CMOS register concept and design master slave triggered register, explain its operation with overlapping periods. (13)

(OR)

b) Explain the memory architecture and its control circuits in detail. (6+7)

14. a) Explain the concept of carry look ahead adder and discuss its types. (6+7)

(OR)

b) Design a multiplier for 5 bit by 3 bit. Explain its operation and summarize the number of adders. Discuss it over Wallace multiplier. (5+4+4)

15. a) Explain the various types of ASIC with neat diagram. (6+7)

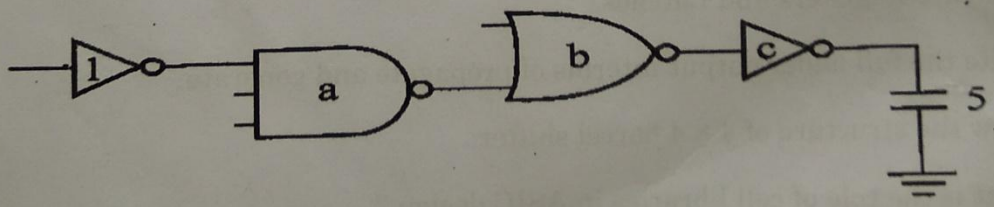
(OR)

b) Draw and explain the building blocks of FPGA. (6+7)

PART – C (1×15=15 Marks)

16. a) i) Design a CMOS logic circuit for the given expression $X = [(A + B).(C + D)]'$ and draw its stick diagram. (7)

ii) Obtain the logical effort and path efforts of the given circuit. (8)



(OR)

b) i) Design a clock distribution network based on H tree model for 16 nodes. (7)

ii) Design a four input NAND gate and obtain its delay during the transition from high to low. (8)

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85

Question Paper Code : 50447

B.E./B.Tech. DEGREE EXAMINATION, NOVEMBER/DECEMBER 2017

Sixth/Seventh/Eighth Semester

Electronics and Communication Engineering

EC 6601 : VLSI DESIGN

(Common to Biomedical Engineering/Electrical and Electronics Engineering/ Electronics and Instrumentation Engineering/Medical Electronics Engineering/ Robotics and Automation Engineering)

(Regulations 2013)

Time : Three Hours

Maximum : 100 Marks

Answer ALL questions

PART – A

(10×2=20 Marks)

1. Why nMOS transistor is selected as pull down transistor ?
2. What is the need of demarcation line ?
3. Define Elmore's constant.
4. List the types of power dissipation.
5. What is NORA CMOS ?
6. Define clock jitter.
7. How to design a high speed adder ?
8. What is latency ?
9. What is ULSI ?
10. Write the various ways of routing procedure.

50447

PART – B (5×16=80 Marks)

11. a) i) Explain the electrical properties of CMOS. (8)

ii) Discuss the scaling principles and its limits. (8)

(OR)

b) Write the layout design rules and draw diagram for four input NAND and NOR gate. (16)

12. a) i) Draw the CMOS logic circuit for the Boolean expression $Z = [A(B + C) + DE]'$ and explain. (8)

ii) Explain the basic principle of transmission gate in CMOS design. (8)

(OR)

b) i) Explain the domino logic with neat diagram. (8)

ii) Discuss the low power design principles in detail. (8)

13. a) Discuss about the design of sequential dynamic circuits and its pipelining concept. (16)

(OR)

b) Explain the timing basics and clock distribution techniques in synchronous design in detail. (16)

14. a) Draw the structure of ripple carry adder and explain its operation. How the drawback in ripple carry adder overcome by carry look ahead adder and discuss. (16)

(OR)

b) Design a multiplier for 5 bit by 3 bit. Explain its operation and summarize the number of adders. Discuss it over Wallace multiplier. (16)

15. a) Explain the various types of ASIC with neat diagram. (16)

(OR)

b) Draw and explain the building blocks of FPGA. (16)

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Question Paper Code : 71738

B.E./B.Tech. DEGREE EXAMINATION, APRIL/MAY 2017.

Sixth/Seventh/Eighth Semester

Electronics and Communication Engineering

EC 6601 — VLSI DESIGN

(Common to Biomedical Engineering/B.E. Electrical and Electronics Engineering/ B.E. Electronics and Communication Engineering/B.E. Electronics and Instrumentation Engineering/B.E. Medical Electronics Engineering/ B.E. Robotics and Automation Engineering)

(Regulations 2013)

Time : Three hours Maximum : 100 marks

Answer ALL questions.

PART A — (10 × 2 = 20 marks)

1. What is meant Channel length modulation in NMOS transistors?

2. Define propagation delay of a CMOS inverter.

3. Define Elmore constant.

4. State the advantages of transmission gates.

5. What is meant by pipelining?

6. Compare and contrast synchronous design and asynchronous design.

7. List out the components of data path.

8. Give the application of high speed adder.

9. What is meant by CBIC?

10. Name the elements in a Configuration Logic Block.

PART B — (5 × 16 = 80 marks)

11. (a) (i) Draw and explain the DC and transfer characteristics of a CMOS inverter with necessary conditions for the different regions of operation. (8)

(ii) Draw the layout diagram for NAND and NOR gate. (8)

Or

(b) Explain the need of scaling, scaling principles and fundamental units of CMOS inverter. (16)

12. (a) (i) Explain about DCVSL logic with suitable example. (10)

(ii) What is transmission gate? Explain the use of transmission gate. (6)

Or

(b) Explain the static and dynamic power dissipation in CMOS circuits with necessary diagrams and expressions. (16)

13. (a) (i) Explain the operation of True Single Phase Clocked Register. (8)

(ii) Draw and explain the operation of Conventional, pulsed and resettable latches. (8)

Or

(b) Explain the concept of timing issues and pipelining. (16)

14. (a) (i) Explain the concept of carry look ahead adder with neat diagram. (10)

(ii) Discuss the details about speed and area trade off. (6)

Or

(b) Explain the concept of modified Booth multiplier with a suitable example. (16)

15. (a) Explain about different types of ASIC with neat diagram. (16)

Or

(b) (i) Explain about building block architecture of FPGA. (10)

(ii) Write short notes on routing procedures involved in FPGA interconnect. (6)

Reg. No. :

Question Paper Code : 80346

B.E./B.Tech. DEGREE EXAMINATION, NOVEMBER/DECEMBER 2016.

Sixth Semester

Medical Electronics

EC 6601 — VLSI DESIGN

(Common to Electronics and Communication Engineering and also Common to Seventh Semester for Biomedical Engineering Electronics and Instrumentation Engineering and Robotics and Automation Engineering)

(Regulations 2013)

Time : Three hours

Maximum : 100 marks

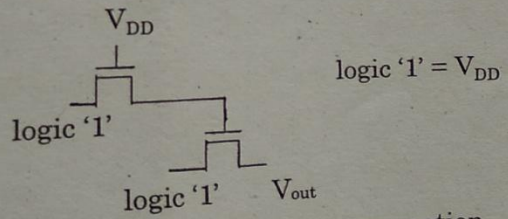
Answer ALL questions.

PART A — (10 × 2 = 20 marks)

1. Define body bias effect.

2. Draw the stick diagram and layout for CMOS inverter.

3. What is the value of V_{out} for the figure shown below, where V_{tn} is threshold voltage of transistor?



4. List out the sources of static and dynamic power consumption.

5. What is meant by pipelining?

6. Draw the schematic of dynamic edge-triggered register.

7. Why is barrel shifter very useful in the designing of arithmetic circuits?

8. Write the principle of any one fast multiplier?

9. What is the standard cell-based ASIC design?

10. What is an antifuse? State its merits and demerits.

PART B — (5 × 16 = 80 marks)

11. (a) (i) Explain the different steps involved in n-well CMOS fabrication process with neat diagrams. (12)

(ii) Derive the noise margins for a CMOS inverter. (4)

Or

(b) (i) Discuss in detail with a neat layout, the design rules for a CMOS inverter. (8)

(ii) Discuss the mathematical equations that can be used to model the drain current and diffusion capacitance of MOS transistors. (8)

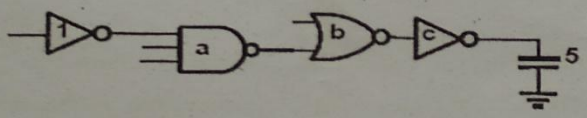
12. (a) Write short notes on :

(i) Ratioed Circuits (8)

(ii) Dynamic CMOS Circuits. (8)

Or

(b) (i) Estimate least delay and determine input capacitance of each stages for the logic network shown in figure, which may represent the critical path of a more complex logic block. The output of the network is loaded with a capacitance which is 5 times larger than the input capacitance of the first gate, which is a minimum-sized inverter. (8)



(ii) Explain the dynamic power dissipation in CMOS circuits with necessary diagrams and expressions. (8)

13. (a) Discuss in detail various static latches and registers. (16)

Or

(b) Write short notes on :

(i) True single-phase clocked register (8)

(ii) NORA – CMOS latches. (8)

14. (a) Explain the operation of a basic 4 bit adder, Describe the different approaches of improving the speed of the adder. (16)

Or

(b) Explain the operation of booth multiplication with suitable examples? Justify how booths algorithm speed up the multiplication process. (16)

15. (a) Discuss the different types of programming technology used in FPGA design. (16)

Or

(b) Briefly explain the semi custom ASIC with its classification. (16)

Reg. No. | | | | | | | | | | | | |

Question Paper Code : 57297

B.E/B.Tech. DEGREE EXAMINATION, MAY/JUNE 2016

Sixth Semester

MEDICAL ELECTRONICS

EC 6601 – VLSI DESIGN

(Common to Electronics and Communication Engineering

(Regulations 2013)

Time : Three Hours **Maximum : 100 Marks**

Answer ALL questions.

PART – A (10 × 2 = 20 Marks)

1. State channel-length modulation. Write down the equation for describing the channel length modulation effect in NMOS transistors.
2. What is Latch-up ? How to prevent latch up ?
3. Give Elmore delay expression for propagation delay of an inverter.
4. Why single phase dynamic logic structure cannot be cascaded ? Justify.
5. Draw the switch level schematic of multiplexer based nMOS latch using nMOS only pass transistors for multiplexers.
6. What is clocked CMOS register ?
7. What is meant by bit-sliced data path organization ?
8. Determine propagation delay of n-bit carry select adder.
9. What are feed-through cells ? State their uses.
10. State the features of full custom design.

PART – B (5 × 16 = 80 Marks)

11. (a) (i) Describe the equation for source to drain current in the three regions of operation of a MOS transistor and draw the VI characteristics. **(8)**

(ii) Explain in detail about the body effect and its effect in MOS device. **(8)**

OR

(b) (i) Explain the DC transfer characteristics of a CMOS Inverter with necessary conditions for the different regions of operation. **(8)**

(ii) Discuss the principles of constant field and lateral scaling. Write the effects of the above scaling methods on the device characteristics. **(8)**

12. (a) (i) Draw the static CMOS logic circuit for the following expression **(8)**

(a) $Y = \left(\overline{A \cdot B \cdot C \cdot D}\right)$

(b) $Y = \overline{D(A + BC)}$

(ii) Discuss in detail the characteristics of CMOS transmission gate ? **(8)**

OR

(b) What are the sources of power dissipation in CMOS and discuss various design techniques to reduce power dissipation in CMOS ? **(16)**

13. (a) Explain the operation of master-slave based edge triggered register. **(16)**

OR

(b) Discuss in detail various pipelining approaches to optimize sequential circuits. **(16)**

14. (a) Design a 16 bit carry bypass and carry select adder and discuss their features. **(8 + 8)**

OR

(b) Design a 4 × 4 array multiplier and write down the equation for delay. **(16)**

15. (a) With neat sketch explain the CLB, IOB and programmable interconnects of an FPGA device. **(16)**

OR

(b) Write brief notes on :

(a) Full custom ASIC **(8)**

(b) Semi custom ASIC **(8)**
