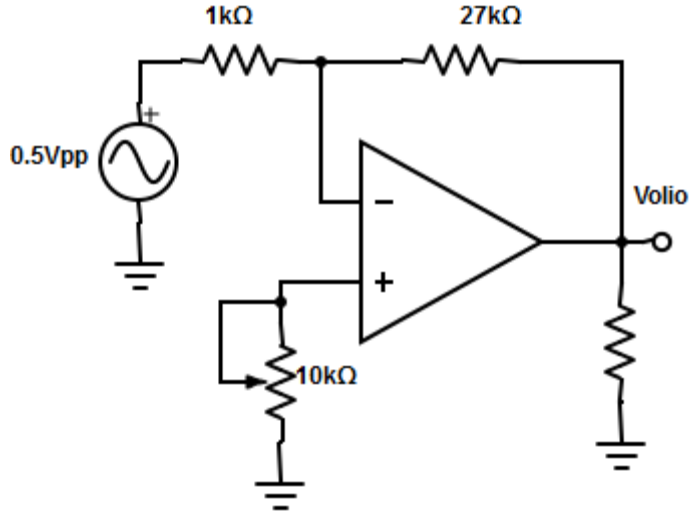
GRT INSITITUTE OF ENGINEERING AND TECHNOLOGY –TIRUTTANI – 631209

EC8453 LINEAR INTEGRATED CIRCUITS (Regulation 2017)
MCQ

1. Open loop op-amp configuration has
   a) Direct network between output and input terminals
   b) No connection between output and feedback network
   c) No connection between input and feedback network
   d) All of the mentioned
2. In which configuration does the op-amp function as a high gain amplifier?
   a) Differential amplifier
   b) Inverting amplifier
   c) Non-inverting amplifier
   d) All of the mentioned
3. The output voltage of an open-loop differential amplifier is equal to
   a) Double the difference between the two input voltages
   b) Product of voltage gain and individual input voltages
   c) Product of voltage gain and the difference between the two input voltages
   d) Double the voltage gain and the difference between two input voltages
4. Find the output of inverting amplifier?
   a) $V_o = AV_{in}$
   b) $V_o = -AV_{in}$
   c) $V_o = -A(V_{in1} – V_{in2})$
   d) None of the mentioned
5. Which of the following electrical characteristics is not exhibited by an ideal op-amp?
   a) Infinite voltage gain
   b) Infinite bandwidth
   c) Infinite output resistance
   d) Infinite slew rate
6. Find the input voltage of an ideal op-amp. It's one of the inputs and output voltages are 2v and 12v. (Gain=3)
   a) 8v
   b) 4v
   c) -4v
   d) -2v
7. Input bias current is defined as
   a) Average of two input bias current
   b) Summing of two input bias current
   c) Difference of two input bias current
   d) Product of two input bias current
8. The formula for output offset voltage of an op-amp due to input bias current
   a) $V_{OIB} = R_F * I_B$
   b) $V_{OIB} = (R_F + R_1)/I_B$
   c) $V_{OIB} = (1+R_F) * I_B$
   d) $V_{OIB} = [1+(R_F/R_1)] * I_B$
9. Which factor affect the input offset voltage, bias current and input offset current in an op-amp
   a) Change in temperature
   b) Change in supply voltage
   c) Change in time
   d) All of the mentioned

10. Determine the maximum output offset voltage caused by input offset current



a) 5.4mv
b) 7.3mv
c) 6.9mv
d) 8.1mv

11. A completely compensated inverting amplifier is nulled at room temperature 25°C, determine the temperature at which the total output offset voltage will be zero?
a) 50°C
b) 25°C
c) 75°C
d) 125°C

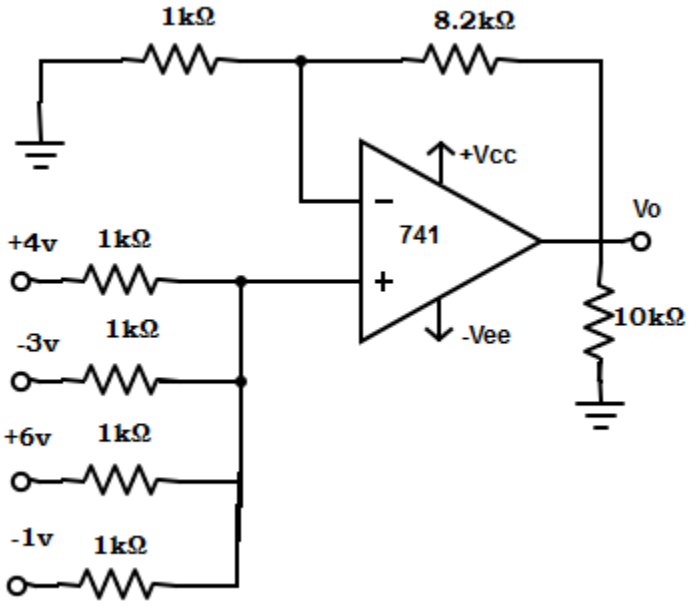
12. Slew rate is defined as the rate of change of
a) Output voltage with respect to time
b) Input voltage with respect to time
c) Both output input voltage with respect to time
d) None of the mentioned

13. How the slew rate is represented?
a) 1V/ms
b) 1V/s
c) 1V/µs
d) 1mv/S

13. Which type of amplifier has output voltage equal to the average of all input voltages?
a) Inverting averaging amplifier
b) Non-inverting averaging amplifier
c) Non-inverting summing amplifier
d) Inverting scaling amplifier

14.Expression for output voltage of non-inverting summing amplifier with five input voltage?
a) $V_o = 5\times(V_a + V_b + V_c + V_d + V_e)$
b) $V_o = [1+(R_f/R_1)]\times (V_a + V_b + V_c + V_d + V_e)$
c) $V_o = V_a + V_b + V_c + V_d + V_e$
d) $V_o = (V_a + V_b + V_c + V_d + V_e) /5$

15. Find the value of V_1 in the circuit shown below?



a) 4v
b) 2v
c) 3v
d) None of the mentioned

16. An instrumentation system does not include
a) Transducer
b) Instrumentation amplifier
c) Automatic process controller
d) Tester

17. In an instrumentation amplifier using transducer bridge, which device measure the change in physical energy
a) Resistive transducer
b) Indicating meter
c) Capacitive transducer
d) Inductor circuit

18.Which of the following functions does the antilog computation required to perform continuously with log-amps?
a) In(x)
b) log(x)
c) Sinh(x)
d) All of the mentioned

19.Find the output voltage of the log-amplifier
a) $V_O = -(kT)\times\ln(V_i/V_{ref})$
b) $V_O = -(kT/q)\times\ln(V_i/V_{ref})$
c) $V_O = -(kT/q)\times\ln(V_{ref}/V_i)$
d) $V_O = (kT/q)\times\ln(V_i/V_{ref})$

20. The circuit in which the output voltage waveform is the integral of the input voltage waveform is called
a) Integrator
b) Differentiator
c) Phase shift oscillator
d) Square wave generator

21. Why practical integrator is called as lossy integrator?
a) Dissipation power
b) Provide stabilization
c) Changes input
d) None of the mentioned

22. Differentiation amplifier produces
a) Output waveform as integration of input waveform

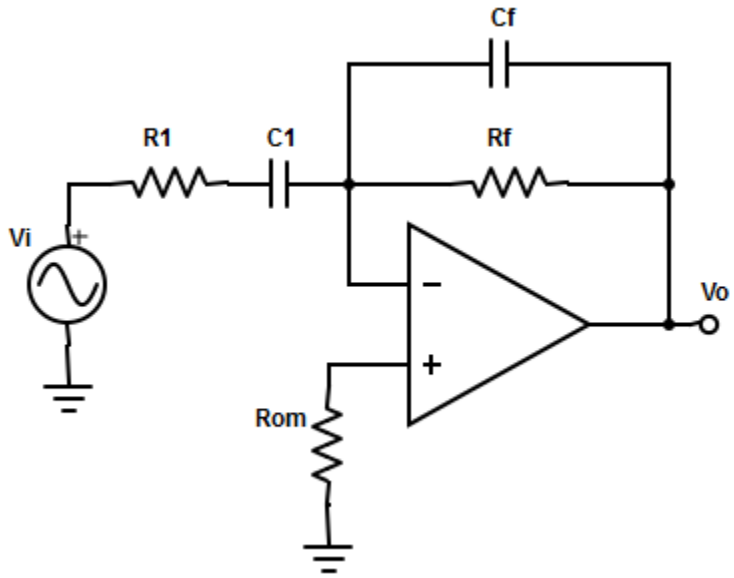
b) Input waveform as integration of output waveform
c) Output waveform as derivative of input waveform
d) Input waveform as derivative of output waveform

23. 3. Determine the output voltage of the differentiator?
a) $V_O = R_F \times C_1 \times [dV_{in}/dt]$.
b) $V_O = -R_F \times C_1 \times [dV_{in}/dt]$.
c) $V_O = R_F \times C_F \times [dV_{in}/dt]$.
d) None of the mentioned

24. which factor makes the differentiator circuit unstable?
a) Output impedance
b) Input voltage
c) Noise
d) Gain

25. Which application use differentiator circuit?
a) None of the mentioned
b) FM modulators
c) Wave generators
d) Frequency Shift keying

26. Determine the transfer function for the practical differentiator



a) $V_o(s)/V_1(s) = -S \times R_F \times C_1/(1+R_1 \times C_1)^2$
b) $V_o(s)/V_1(s) = -S \times R_F \times C_1/(1+R_F \times C_1)^2$
c) $V_o(s)/V_1(s) = -S \times R_F \times C_1/(1+R_1 \times C_F)^2$
d) None of the mentioned

27. Filters are classified as
a) Analog or digital
b) Passive or active
c) Audio or radio frequency
d) All of the mentioned

28. The problem of passive filters is overcome by using
a) Analog filter
b) Active filter
c) LC filter
d) A combination of analog and digital filters

29. Find out the incorrect statement about active and passive filters.
a) Gain is not attenuated in active filter
b) Passive filters are less expensive
c) Active filter does not cause loading of source
d) Passive filters are difficult to tune or adjust

30. Choose the op-amp that improves the filter performance.
a) µA741

b) LM318
c) LM101A
d) MC34001

31. Which filter type is called a flat-flat filter?
a) Cauer filter
b) Butterworth filter
c) Chebyshev filter
d) Band-reject filter

32. Which filter performs exactly the opposite to the band-pass filter?
a) Band-reject filter
b) Band-stop filter
c) Band-elimination filter
d) All of the mentioned

33. Given the lower and higher cut-off frequency of a band-pass filter are 2.5kHz and 10kHz. Determine its bandwidth.
a) 750 Hz
b) 7500 Hz
c) 75000 Hz
d) None of the mentioned

34. Name the filter that has two stop bands?
a) Band-pass filter
b) Low pass filter
c) High pass filter
d) Band-reject filter

35. The frequency response of the filter in the stop band.
i. Decreases with increase in frequency
ii. Increase with increase in frequency
iii. Decreases with decrease in frequency
iv. Increases with decrease in frequency
a) i and iv
b) ii and iii
c) i and ii
d) ii and iv

36. Determine output voltage of analog multiplier provided with two input signal Vx and Vy.
a) $V_o = (V_x \times V_y) / V_{ref2}$
b) $V_o = (V_x \times V_x) / V_y$
c) $V_o = (V_x \times V_y / V_{ref}$
d) $V_o = (V_y \times V_y) / V_{xSNI}$

37. Which circuit allows to double the frequency?
a) Frequency doubler
b) Square doubler
c) Double multiplier
d) All of the mentioned

38. How to remove the dc term produced along with the output in frequency doubler?
a) Use a Inductor between load and output terminal
b) Use a capacitor between load and output terminal
c) Use a potentiometer between load and output terminal
d) Use a resistor between load and output terminal

39. Which circuit can be used to take square root of a signal?
a) Divider circuit
b) Multiplier circuit
c) Squarer circuit
d) None of the mentioned

40. The output frequency of the VCO can be changed by changing
a) External tuning resistor

b) External tuning capacitor
c) Modulating input voltage
d) All of the mentioned

41. What is the advantage of using filter in PLL?
a) High noise immunity
Reduce the bandwidth of PLL
Provides dynamic range of frequencies
None of the mentioned

42. Voltage to frequency conversion factor for VCO is
a) $K_v = \Delta f_o/\Delta V_c$
b) $K_v = \Delta f_o \times \Delta V_c$
c) $K_v = 1/(\Delta f_o \times \Delta V_c)$
d) $K_v = \Delta V_c/ \Delta f_o$

43. The output voltage of phase detector is
a) Phase voltage
b) Free running voltage
c) Error voltage
d) None of the mentioned

44. At which state the phase-locked loop tracks any change in input frequency?
a) Free running state
b) Capture state
c) Phase locked state
d) All of the mentioned

45. What is the need to generate corrective control voltage?
a) To maintain the lock
b) To track the frequency change
c) To shift the VCO frequency
d) All of the mentioned

46. The practical use of binary-weighted digital-to-analog converters is limited to
a) 4-bit D/A converter
b) 8-bit D/A converter
c) R-2R Ladder D/A converter
d) op-amp comparator

47. In a flash analog-to-digital converter, the output of each comparator is connected to an input of a
a) demultiplexer
b) multiplexer
c) priority encoder
d) decoder

48. What is the resolution of a digital-to-analog converter (DAC)?
a) It is its ability to resolve between forward and reverse steps when sequenced over its entire range.
b) It is the smallest analog output change that can occur as a result of an increment in the digital input.
c) It is the comparison between the actual output of the converter and its expected output.
d) It is the deviation between the ideal straight-line output and the actual output of the converter.

49. Which is not an analog-to-digital (ADC) conversion error?
a) missing code
b) incorrect code
c) differential nonlinearity
d) offset

50. A digital voltmeter uses a
a) Sigma-Delta ADC

b) Successive approximation type ADC
c) Dual slope ADC
d) flash ADC

51. Express the output voltage of digital to analog converter?
a) $V_o = V_{FS}/k(d_1 2^{-1}+d_2 2^{-2}+\ldots d_n 2^{-n})$
b) $V_o = KV_{FS}(d_1 2^{-1}+d_2 2^{-2}+\ldots d_n 2^{-n})$
c) $V_o = V_{FS}(d_1 2^{-1}+d_2 2^{-2}+\ldots d_n 2^{-n})$
d) $V_o = K(d_1 2^{-1}+d_2 2^{-2}+\ldots d_n 2^{-n})$

52. Why the switches used in weighted resistor DAC are of single pole double throw (SPDT) type?
a) To connect the resistance to either reference voltage or ground
b) To connect the resistance to output
c) To connect the resistance to reference voltage
d) To connect the resistance to ground

53. In a D-A converter with binary weighted resistor, a desired step size can be obtained by
a) Selecting proper value of V_{FS}
b) Selecting proper value of R
c) Selecting proper value of R_F
d) All of the mentioned

54. Which type of switches are not preferable for a simple weighted resistor DAC?
a) Bipolar Transistor
b) Voltage switches
c) MOSFET
d) All of the mentioned

55. The inverted R-2R ladder can also be operated in
a) Current Mode
b) Voltage mode
c) Inverted mode
d) Non inverted mode

56. Which of among the following circuit is considered to be linear?
a) Weighted Resistor type DAC
b) R-2R ladder type DAC
c) Inverter R-2R ladder DAC
d) All of the mentioned

57. How to overcome the limitation of binary weighted resistor type DAC?
a) Using monolithic DAC
b) Multiplying DACs
c) Using hybrid DAC
d) Using R-2R ladder type DAC

58. A multiplying DAC is given a reference voltage VR = Vom cos2πft. Determine the output voltage?
a) $V_o(t) = V_{om} \sec(2\pi ft+180^o)$
b) $V_o(t) = V_{om} \cos(2\pi ft+180^o)$
c) $V_o(t) = V_{om} \tan(2\pi ft+180^o)$
d) $V_o(t) = V_{om} \sin(2\pi ft+180^o)$

59. Find out the resolution of 8 bit DAC/ADC?
a) 562
b) 625
c) 265
d) 256

60. A binary input 000 is fed to a 3bit DAC/ADC. The resultant output is 101. Find the type of error?
a) Linearity error

b) Offset error
c) Gain error
d) Settling error

61. A monotonic DAC is one whose analog output increases for
a) Decreases in analog input
b) An increases in analog input
c) Decreases in digital input
d) An increases in digital input

62. The time taken for the output to settle within a specified band of its final value is referred as
a) Conversion time
b) Settling time
c) Take off time
d) All of the mentioned

63. How many control lines are present in analog to digital converter in addition to reference voltage?
a) Three
b) Two
c) One
d) None of the mentioned

64. Sample-and-hold circuits in analog-to digital converters (ADCs) are designed to:
a) sample and hold the D/A converter staircase waveform during the conversion process
b) stabilize the input analog signal during the conversion process
c) sample and hold the output of the binary counter during the conversion process
d) stabilize the comparator's threshold voltage during the conversion process

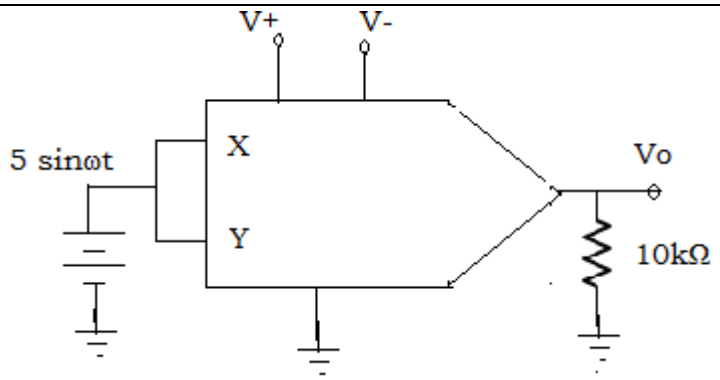
65. The primary disadvantage of the flash analog-to digital converter (ADC) is that
a) A large number of output lines is required to simultaneously decode the input voltage
b) A large number of comparators is required to represent a reasonable sized binary number
c) A long conversion time is required
d) It requires the input voltage to be applied to the inputs simultaneously

66. Match the list-I with list-II

List-I	List-II
1. One quadrant multiplier	i. Input 1- Positive, Input 2- Either positive or negative
2. Two quadrant multiplier	ii. Input 1- Positive, Input 2 – Positive
3. Four quadrant multiplier	iii. Input 1- Either positive or negative, Input 2- Either positive or negative

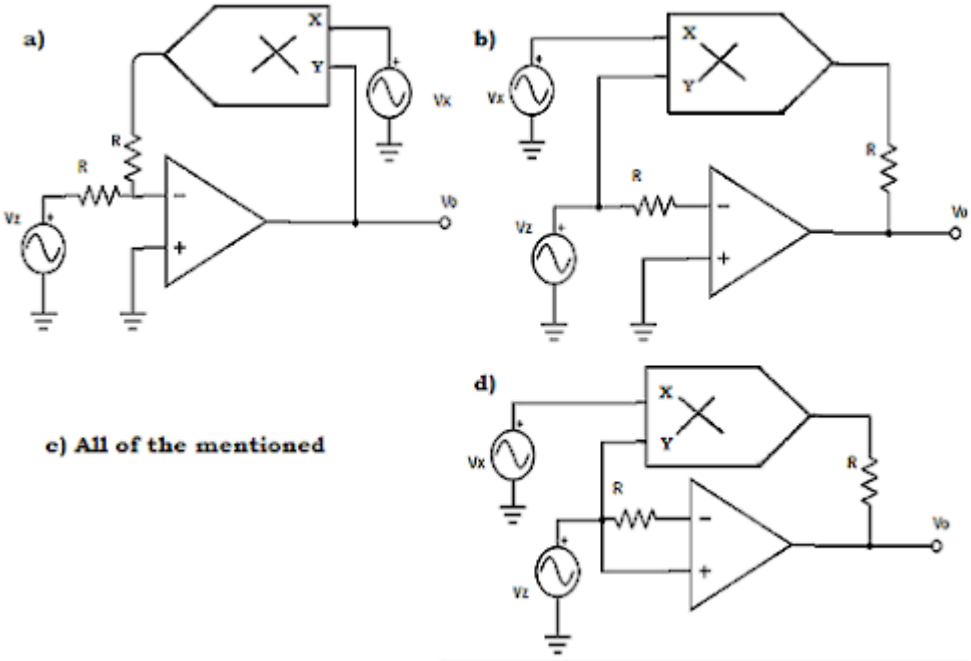
a) 1-i, 2-ii, 3-iii
b) 1-iii, 2-i, 3-ii
c) 1-ii, 2-iii, 3-i
d) 1-ii, 2-i, 3-iii

67. Find the output voltage for the squarer circuit given below, choose input frequency as 10kHz and V_{ref} =10v



a) V_o = 5.0-(5.0×cos4π×104t)
b) V_o = 2.75-(2.75×cos4π×104t)
c) V_o = 1.25-(1.25×cos4π×104t)
d) None of the mentioned

68. Find the divider circuit configuration given below



c) All of the mentioned

a) a
b) c
c) b
d) d

69. How to obtain a desired amount of multiplication in frequency multiplier?
a) By decreasing the multiplication factor
b) By increasing the input frequency
c) By selecting proper divide by N-network
d) None of the mentioned

70. Calculate the output frequency in a frequency multiplier if, fin = 200Hz is applied to a 7 divide by N-network.
a) 1.2kHz
b) 1.6kHz
c) 1.4kHz
d) 1.9kHz

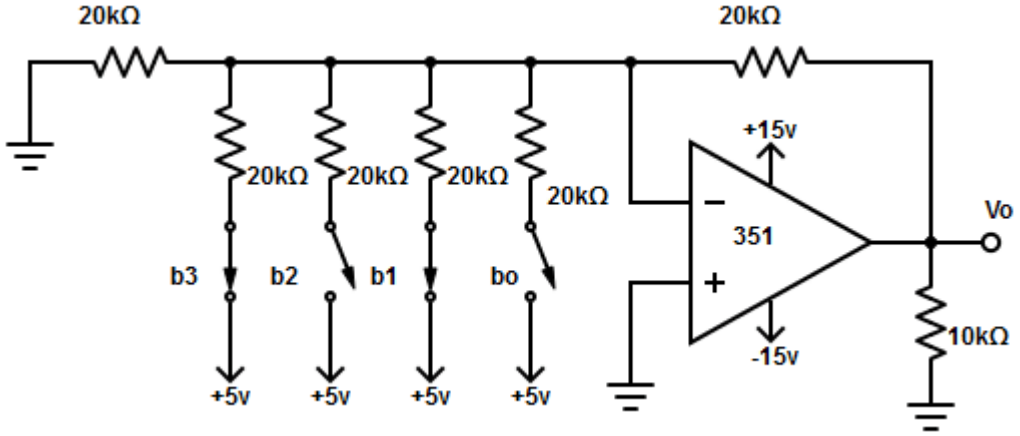
71. Match the list I with list II which represents the three stages of phase locked loop.(PLL)

List I	List II
1.Before input frequency	i. PLL-Phase locked applied state
2.When the input frequency	ii.PLL=Free running applied state
3.After input frequency	iii. PLL-Capture mode applied

a) 1-ii, 2-iii, 3-i
b) 1-i, 2-ii, 3-iii
c) 1-ii, 2-i, 3-iii
d) 1-iii, 2-ii, 3-i

72. Determine the value of current flow in VCO, when the NE566 VCO external timing resistor RT =250Ω and the modulating input voltage Vc=3.25V.(Assume Vcc=+5v).
a) 7mA
b) 3mA
c) 12mA
d) 10mA

73. For the given circuit find the output voltage?



a) -3.125v
b) -4.375v
c) -3.50v
d) -5.625v

74. A 10-bit D/A converter have an output range from 0-9v. Calculate the output voltage produced when the input binary number is 1110001010.
a) ±7.96v
b) -7.96v
c) 7.96v
d) None of the mentioned

75. How many equal intervals are present in a 14-bit D-A converter?
a) 4095
b) 65535
c) 1023
d) 16383

76. Determine the offset frequency of frequency translation, when the output and input frequency are given as 75kHz and 1000Hz.
a) 14 kHz
b) 20 kHz
c) 29 kHz
d) 35 kHz

77. When a PLL is being used for FM modulation, the demodulated signal appears at __
    a) Output of LPF
    b) Output of VCO
    c) Input of phase comparator
    d) none

78. When a PLL is being used for Frequency synthesizer, the output is taken from
    a) Output of error amplifier
    b) Output of LPF
    c) Output of phase comparator
    d) Output of VCO

79. The pull-in time of PLL depends on
    a) Initial phase and frequency difference between two sign
    b) Overall loop gain
    c) Loop filter characteristics
    d) All of the mentioned

80. What happens when VCO output is 90o out of phase with respect to input signal?
    a) Error signal is removed
    b) Attenuation
    c) Shift in phase of comparator
    d) Perfect lock

81. What will be the phase shift of feedback circuit in RC phase shift oscillator?
    a) 360^o phase shift
    b) 180^o phase shift
    c) 90^o phase shift
    d) 60^o phase shift

82. Calculate the frequency of oscillation for RC phase shift oscillator having the value of R and C as 35Ω and 3.7μF respectively.
    a) 1230 Hz
    b) 204 Hz
    c) 502Hz
    d) 673 Hz

83. The condition for zero phase shift in wein bridge oscillator is achieved by
    a) Connecting feedback to non-inverting input terminal of op-amp
    b) Balancing the bridge
    c) Applying parallel combination of RC to the feedback network
    d) All of the mentioned

84. Determine the expression for time period of a square wave generator
    a) $T= 2RC \ln\times[(R_1+ R_2) / (R_2)]$.
    b) $T= 2RC \ln\times[(2R_1+ R_2) / (R_2)]$.
    c) $T= 2RC \ln\times[(R_1+ 2R_2) / (R_2)]$.
    d) $T= 2RC \ln\times[(R_1+ R_2) / (2 R_2)]$.

85. What will be the frequency of output waveform of a square wave generator if $R_2 = 1.16 R_1$?
    a) $f_o = (1/2RC)$
    b) $f_o = (\ln/2RC)$
    c) $f_o = (\ln /2 \times\sqrt{RC})$
    d) $f_o = (\ln/\sqrt{(2 RC)})$

86. How a triangular wave generator is derived from square wave generator?
    a) Connect oscillator at the output
    b) Connect Voltage follower at the output
    c) Connect differential at the output
    d) Connect integrator at the output

87. The increase in the frequency of triangular wave generator.
    a) Ramp the amplitude of triangular wave
    b) Increase the amplitude of triangular wave

c) Decrease the amplitude of triangular wave
d) None of the mentioned

88. What is the peak to peak (PP) output amplitude of the triangular wave?
a) $V_O(pp) = + V_{Ramp} + (- V_{Ramp})$
b) $V_O(pp) = - V_{Ramp} + (+ V_{Ramp})$
c) $V_O(pp) = + V_{Ramp} - (- V_{Ramp})$
d) $V_O(pp) = - V_{Ramp} - (+ V_{Ramp})$

89. Find the capacitor value for a the output frequency, f_o = 2kHz & $V_O(pp)$ = 7v, in a triangular wave generator. The op-amp is 1458/741 and supply voltage = ±15v. (Take internal resistor=10kΩ)
a) 0.03nF
b) 30nF
c) 0.3nF
d) 3nF

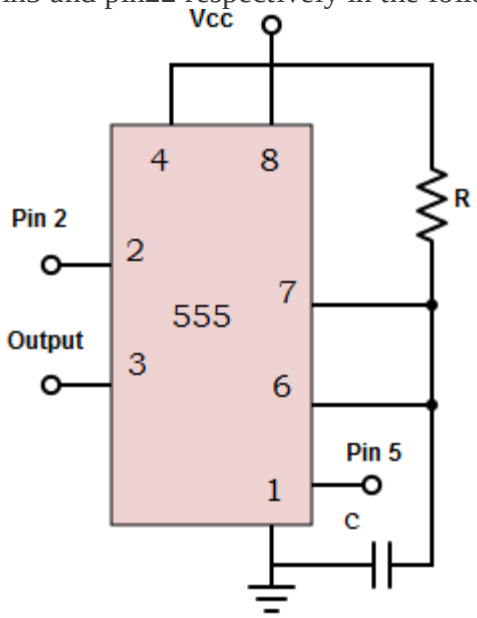
90. Triangular wave form has
a) Rise time < fall time
b) Rise time = fall time
c) Rise time ≥ fall time
d) None of the mentioned

91. Output of an integrator producing waveforms of unequal rise and fall time are called
a) Triangular waveform
b) Sawtooth waveform
c) Pulsating waveform
d) Spiked waveform

92. Determine the time period of a monostable 555 multivibrator.
a) T = 0.33RC
b) T = 1.1RC
c) T = 3RC
d) T = RC

93. A monostable multivibrator has R = 120kΩ and the time delay T = 1000ms, calculate the value of C?
a) 0.9µF
b) 1.32µF
c) 7.5µF
d) 2.49µF

94. What will be the output, if a modulating input signal and continuous triggering signal are applied to pin5 and pin22 respectively in the following circuit?



a) Frequency modulated wave form
b) Pulse width modulated wave form
c) Both pulse and frequency modulated wave form
d) None of the mentioned

95. Free running frequency of Astable multivibrator?
a) $f=1.45/(R_A+2R_B)C$
b) $f=1.45(R_A+2R_B)C$
c) $f=1.45C/(R_A+2R_B)$
d) $f=1.45\ R_A/(\ R_A+R_B)$

96. Astable multivibrator operating at 150Hz has a discharge time of 2.5m. Find the duty cycle of the circuit.
a) 50%
b) 75%
c) 95.99%
d) 37.5%

97. How to achieve 50% duty cycle in adjustable rectangular wave generator? (Assume R_1 –> Resistor connected between supply and discharge and R_2 –> Resistor connected between discharge and trigger input.)
a) $R_1 < R_2$
b) $R_1 > R_2$
c) $R_1 = R_2$
d) $R_1 \geq R_2$

98. How does a monostable multivibrator used as frequency divider?
a) Using square wave generator
b) Using triangular wave generator
c) Using sawtooth wave generator
d) Using sine wave generator

99. Write the equation for time period of VCO?
a) $(2\times V_{cc}\times C_T)/i$
b) $(V_{cc}\ C_T)/(2\times i)$
c) $(V_{cc}\times C_T\times i)/2$
d) $(2\times V_{cc})/(i\times C_T)$

100. Calculate the voltage to frequency conversion factor, where f_o=155Hz and V_{cc}=10V.
a) 130
b) 124
c) 134
d) 116