EC 8453 – Linear Integrated Circuits

Unit 1 : Basics of Operational Amplifier

(1) Constant Current Source [Current mirror]:

A constant current source makes use of the fact that transistor in active mode of operation, V_c is independent of I_c

Ckt: → Transistor Q_1 & Q_2 are matched [∵ fabricated using IC technology]

→ Base and Emitter of Q_1 & Q_2 are tied together So Same V_{BE}

→ Q_1 is connected as diode by shorting collector & base

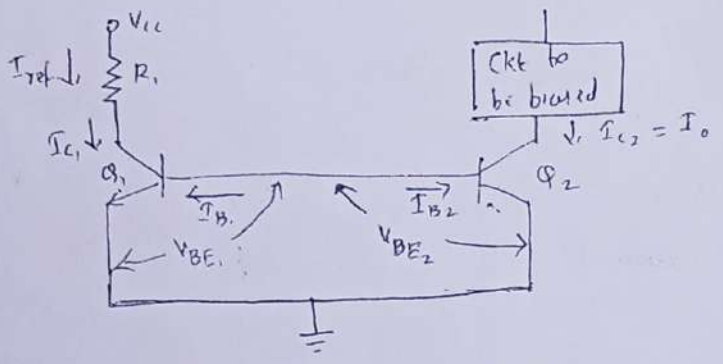


Fig. Basic BJT Current mirror

When i/p current flows through diode connected Q_1 so Base and emitter B-E establishes voltage across Q_1. This voltage appear b/w B-E of Q_2. (Q_2 identical to Q_1)

$$I_E(Q_2) = I_E(Q_1) \approx I_{ref}$$

As long as Q_1 is maintained in active region

$$I_{C_2} = I_o \simeq I_{ref}$$

Since I_o (o/p current) is reflection (or) mirror of the reference current I_{ref}. The circuit is referred to as "current mirror".

Mirror effect valid only for large value of β

Effect of β on the operation of the current mirror ckt. Analysis

collector currents of Q_1 & Q_2 : I_{C1} and I_{C2}

$$I_{C1} \simeq \alpha_F I_{ES} e^{V_{BE1}/V_T} \quad - (1)$$

$$I_{C2} \simeq \alpha_F I_{ES} e^{V_{BE2}/V_T} \quad - (2)$$

From (1) & (2)

$$\frac{I_{C2}}{I_{C1}} = \frac{(\alpha_F I_{ES}) e^{V_{BE2}/V_T}}{(\alpha_F I_{ES}) e^{V_{BE1}/V_T}}$$

$$= \frac{e^{V_{BE2}/V_T}}{e^{V_{BE1}/V_T}} \Rightarrow e^{V_{BE2}/V_T} \cdot e^{-V_{BE1}/V_T}$$

$$\therefore \frac{I_{C2}}{I_{C1}} = e^{(V_{BE2} - V_{BE1})/V_T} \quad - (3)$$

$\because V_{BE2} = V_{BE1}$

$$\Rightarrow I_{C2} = I_{C1} = I_C = I_O$$

Since Q_1 & Q_2 are identical,

$$\boxed{\beta_1 = \beta_2 = \beta}$$

Applying KCL at collector of Q_1,

$$\Rightarrow I_{ref} = I_{C1} + I_{B1} + I_{B2} \quad - (4)$$

$$= I_{C1} + \frac{I_{C1}}{\beta_1} + \frac{I_{C2}}{\beta_2} \quad \left[\because \beta I_B = I_C,\ I_{C1} = I_{C2} = I_C\right]$$

$$= I_C + \frac{I_C}{\beta} + \frac{I_C}{\beta}$$

$$I_{ref} = I_C + \frac{2I_C}{\beta} = I_C\left[1 + \frac{2}{\beta}\right] \quad - (5)$$

Solving (5) $I_C = \left[\beta/\beta + 2\right] I_{ref} \quad - (6)$

From fig I_{ref} is, $I_{ref} = \frac{V_{CC} - V_{BE}}{R_1} = \frac{V_{CC}}{R_1}$ [$\because V_{BE} = 0.7V$ Silicon]

From (6) for $\beta >> 1$, $\beta/(\beta+2)$ is unity and $I_o = I_{ref}$ which for a given R is constant

* Current transfer ratio other than unity by controlling area of the emitter - base Junction [EBJ] of Q_2

Ex: EBJ of Q_2 = 4 times than of Q_1,

$I_o = 4 I_{ref}$

Output resistance of current source is the o/p resistance r_o of Q_2

$$R_o = r_{o_2} = \frac{V_A}{I_o} \simeq \frac{V_A}{I_{ref}}$$

V_A - early voltage

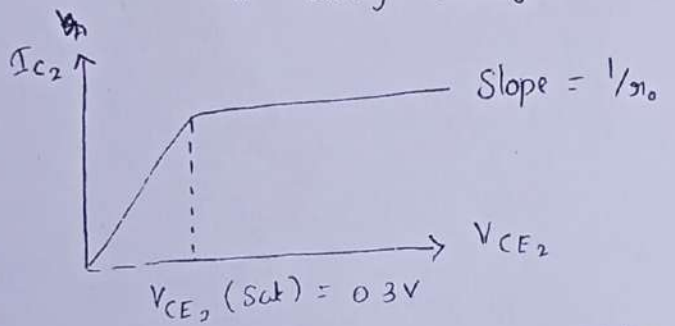


fig. Volt - Ampere characteristics for Q_2

Graph: $V_{CE_2} < 0.3V \Rightarrow Q_2$ is Saturated

for $V_{CE_2} > 0.3V$, transistor operates in active region

I_{C_2} is essentially constant

Slight increase in I_{C_2} due to early effect

For practical purpose, early voltage assumed infinite

$r_o \to \infty$ and I_{C_2} is constant

1.2

WIDLAR CURRENT SOURCE

Op Amp requires very small i/p current

Basic current mirror circuit has a limitation:-

→ when low value current source is needed, value of R_1 is high and can't be fabricated

Hence we go for Widlar current source. It is designed for current values of very low magnitude

Construction:-

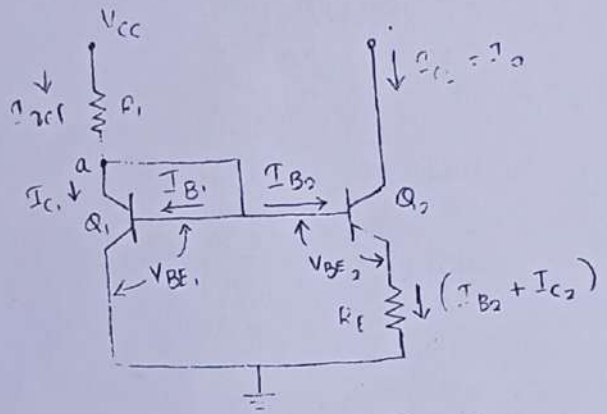


Fig Widlar current source

In this circuit R_E is added to output transistor Q_2 this makes $V_{BE_1} > V_{BE_2}$

Analysis:- Due to R_E, $V_{BE_2} < V_{BE1}$ So, $I_o << I_{C_1}$

$$I_{C_1} = \alpha I_{ES} e^{V_{BE1}/V_T} \rightarrow (1)$$

$$I_{C_2} = \alpha I_{ES} e^{V_{BE2}/V_T} \rightarrow (2)$$

Equating (1) & (2)

$$\frac{I_{C_1}}{I_{C_2}} = e^{(V_{BE_1} - V_{BE2})/V_T} \rightarrow (3)$$

Taking natural logarithm on both sides,

$$\ln \frac{I_{C_1}}{I_{C_2}} = \frac{V_{BE_1} - V_{BE2}}{V_T}$$

$$\therefore V_{BE_1} - V_{BE2} = V_T \ln\left[\frac{I_{C_1}}{I_{C_2}}\right] \rightarrow (4)$$

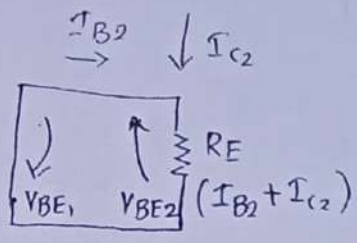
Writing KVL for emitter - base loop of Q_2

$$V_{BE1} = V_{BE2} + (I_{B2} + I_{C2}) R_E$$

$$V_{BE1} - V_{BE2} = (I_{B2} + I_{C2}) R_E \quad \rightarrow (5)$$

$$= \left[\frac{I_{C2}}{\beta} + I_{C2}\right] R_E \quad (\because I_B \beta = I_C)$$

$$= \left(\frac{1}{\beta} + 1\right) I_{C2} R_E \quad \rightarrow (6)$$



From (4) & (6),

$$V_T \ln\left(\frac{I_{C1}}{I_{C2}}\right) = \left(\frac{1}{\beta} + 1\right) I_{C2} R_E$$

$$\therefore \boxed{R_E = \frac{V_T}{\left(1 + \frac{1}{\beta}\right) I_{C2}} \ln\left(\frac{I_{C1}}{I_{C2}}\right)} \quad \rightarrow (7)$$

Relationship between I_{C1} & I_{ref} is obtained by KCL at collector point of Q_1 (node 'a')

$$I_{ref} = I_{C1} + I_{B1} + I_{B2} \quad \rightarrow (8)$$

$$= I_{C1} + \frac{I_{C1}}{\beta} + \frac{I_{C2}}{\beta} \quad (\because I_B \beta = I_C)$$

$$= I_{C1}\left[1 + \frac{1}{\beta}\right] + \frac{I_{C2}}{\beta} \quad \rightarrow (9)$$

For identical transistors, assume $\beta_2 = \beta_1 = \beta$

In Widlar current source, $I_{C2} << I_{C1}$

$\therefore I_{C2}/\beta$ is identified neglected in eqn (9)

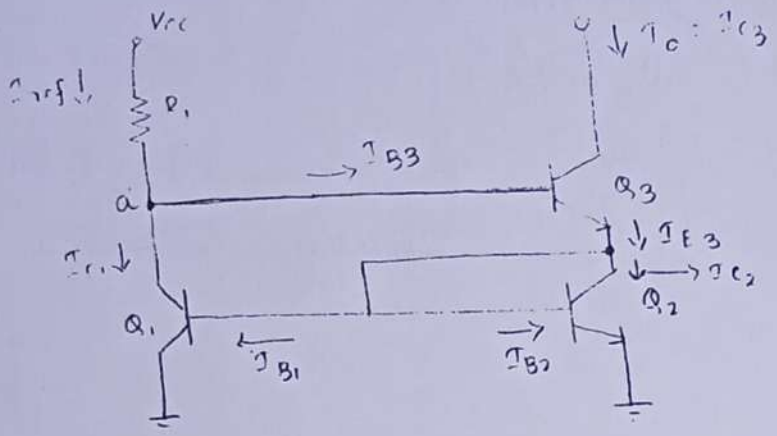
$$\Rightarrow I_{ref} \simeq I_{C1}\left[1 + \frac{1}{\beta}\right]$$

$$I_{C1} = \frac{\beta}{\beta + 1} I_{ref}$$

where, $I_{ref} = \frac{V_{CC} - V_{BE}}{R_1}$

for $\beta >> 1$, $I_{C1} \simeq I_{ref}$

1.1.3 Wilson Current Source:



Construction:-

- It is a 3 terminal ckt that accepts an input current of the input terminal and provides mirror current source
- A mirror current is a copy of input current
- The main feature of Wilson current source is to provide high output resistances with respective high input resistances.
- High output resistance is acheived due to negative feedback through Q_2.

Analysis:-

From fig., $V_{BE1} = V_{BE2}$, $I_{C1} = I_{C2}$ & $I_{B1} = I_{B2} = I_B$

Apply KCL at node 'B', $I_{E3} = I_{C2} + I_{B2} + I_{B1}$

$$I_{E3} = I_{C2} + 2I_{B2} \qquad (\because I_{B1} = I_{B2})$$

$$= I_{C2} + 2\frac{I_{C2}}{\beta}$$

$$= I_{C2}\left[1 + \frac{2}{\beta}\right] \longrightarrow (1)$$

From fig., through Q_3

$$I_{E3} = I_{B3} + I_{C3} \qquad (\because I_E = I_B + I_C)$$

$$= \frac{I_{C3}}{\beta} + I_{C3}$$

$$= I_{C3}\left[\frac{1}{\beta} + 1\right] \longrightarrow (2)$$

From (1) & (2),

$$I_{C2}\left[\frac{\beta+2}{\beta}\right] = I_{C3}\left[\frac{\beta+1}{\beta}\right]$$

$$I_{C3} = \frac{I_{C2}\left[\beta+2/\beta\right]}{} = I_{C2}\left[\frac{\beta+2}{1+\beta}\right]$$

I_{C3} is o/p current I_o, $I_{C2} = I_{C1}$, so I_{C1}

$$\therefore \quad I_o = I_{C1}\left(\frac{\beta+2}{1+\beta}\right)$$

At node 'a': (apply KCL)

$$I_{ref} = I_{C1} + I_{B3}$$
$$= I_o\left[\frac{\beta+1}{\beta+2}\right] + \frac{I_{C3}}{\beta}$$

from $I_{C3} = I_o$

$$I_{ref} = I_o\left[\frac{\beta+1}{\beta+2} + \frac{1}{\beta}\right]$$
$$= I_o\left[\frac{\beta(\beta+1)+\beta+2}{\beta(\beta+2)}\right]$$
$$I_{ref} = I_o\left[\frac{\beta^2+2\beta+2}{\beta^2+2\beta}\right]$$

To find resistance, sub $I_{ref} = \dfrac{V_{CC} - 2V_{BE}}{R_1}$

$$\Rightarrow \frac{V_{CC} - 2V_{BE}}{R_1} = I_o\left[\frac{\beta^2+2\beta+2}{\beta^2+2\beta}\right]$$

R_1 is

The difference, $I_o - I_{ref} = \dfrac{2}{\beta^2+2\beta+2} I_{ref}$

(1.2) Current Source as Active loads:

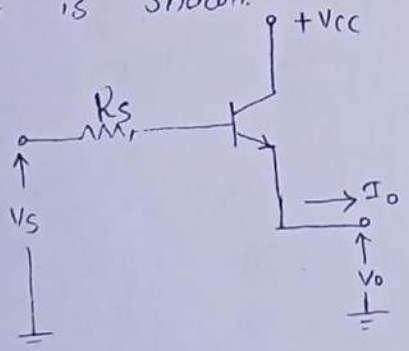
- Current source can be used as an active load in both analog & digital ICs
- The active load realized using "current source" in place of passive load (i.e resistor) in the collector arm of differential amplifier makes it possible to achieve high voltage gain without requiring large power supply voltage
- Active load so achieved is basically "I_o" of a PNP transistor

(1.3) Voltage Sources

- Voltage source is a circuit that produces an output voltage V_o, which is independent of the load driven by the voltage source / output current supplied to the load.
- Voltage source circuit = dual of constant current source
- Application: require voltage reference point with low AC impedance, stable DC voltage not affected by power supply
- Two methods to produce voltage source
  - → using the impedance transforming properties of transistor, determines current gain of transistor
  - → using an amplifier with negative feedback

1.3.1. Voltage Source circuit using Impedance transformation:

- Voltage source circuit using impedance transforming property of transistor is shown.



- Voltage source V_s derives the base of the transistor through series resistance R_s and output is taken across the emitter
- From ckt, output AC resistance looking into emitter given by

$$\frac{dV_o}{dI_o} = R_o = \frac{R_S}{\beta+1} + r_{eb} \longrightarrow (1)$$

with values as high as 100 for β

$$R_S = \frac{R_S}{\beta+1}$$

- Equation is "applicable only for small changes" in the e/p current

- The load regulation parameter indicates the changes in V_o resulting from large changes in o/p current I_o
- Reduction in V_o occurs as I_o goes from no-load current to full-load current. This determines o/p independance of voltage sources

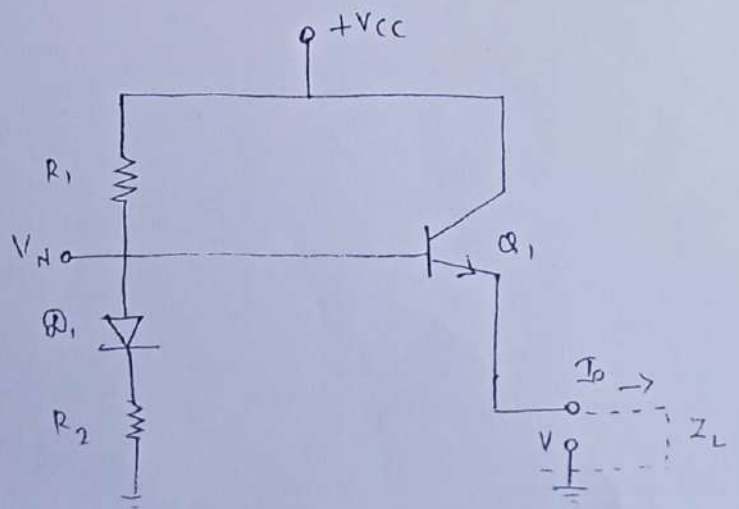
1.3.2 Emitter follower / common collector type voltage source:

- It is suitable for differential gain stage used in op-amp. It has a advantage of
  - → producing low AC impedance
  - → resulting in effective decoupling of adjacent gain stages
- Low o/p impedance of the common collector stage simulates a low impedance voltage source with an o/p voltage level of V_o.

$$V_o = V_{cc}\left[\frac{a_2}{R_1 + R_2}\right]$$

- Diode 'D_1' used for offsetting the effect of dc value V_{BE} and compensating temperature dependance of V_{BE} drop of Q_1.
  X_L = dotted line shows ckt is biased by current through Q_1
- Impedance R_o looking at emitter of Q_1 derived from hybrid π model

$$R_o = \frac{V_T}{I_1} + \frac{R_1 R_2}{\beta R_1 + R_2} C$$



Voltage Source temperature compensated avalanche diode

$$V_o = V_B + V_{BE}$$

The o/p resistance R_o is given as

$$R_o = R_B + \frac{V_T}{I_1}$$

Voltage source using V_{BE} as reference

$$V_o = I_2 (R_1 + R_2) = \frac{V_{BE}}{R_2} (R_1 + R_2) = V_{BE} \left(\frac{R_1}{R_2} + 1 \right)$$

The ac o/p resistance R_o is

$$R_o = \frac{dV_o}{dI_o} = \frac{R_1 + R_2}{1 + g_m R_2}$$

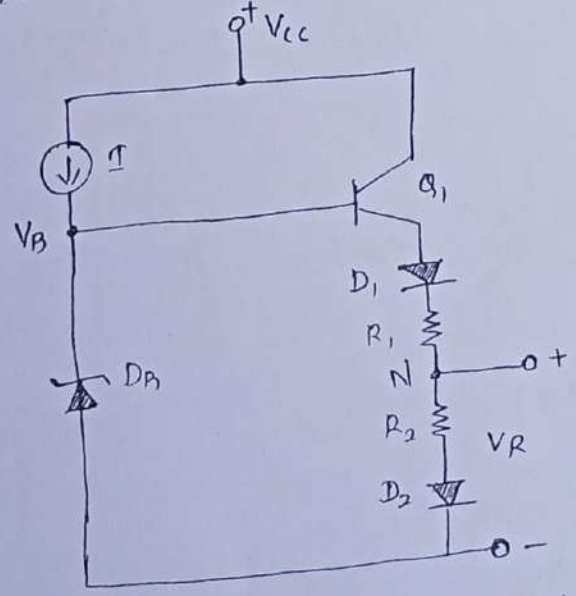
(1.4) VOLTAGE REFERENCES:

- The ckt that is primarily designed for providing constant voltage independent of changes in temperature is called "Voltage reference."
- Important characteristics of voltage reference is temperature co-efficient of o/p reference voltage, T_{CR}

$$T_{CR} = dV_R / dT$$

- Desirable properties of V.R. are
(a) Reference voltage must be independent of temperature change.
(b) Reference voltage must have good power supply rejection which is independent of supply voltage as possible.
(c) o/p voltage must be as independent of the loading of o/p current.

(A) Voltage ref. ckt using Temperature Compensation Scheme:-



Voltage ref. ckt using basic temperature compensation is shown above. Constant current 'I' is supplied to avalanche diode D_B to provide bias voltage V_B to base of Q_1.

Apply KCL at node 'N'

$$\frac{V_B - V_{BE}(Q_1) - V_{BE}(D_1) - V_R}{R_1} = \frac{V_R - V_{BE}(D_2)}{R_2}$$

Assume matched transistors,

$$V_{BE}(Q_1) = V_{BE}(D_1) = V_{BE}(D_2) = V_{BE}$$

Then, V_B :

$$\frac{V_B - 2V_{BE} - V_R}{R_1} = \frac{V_R - V_{BE}}{R_2}$$

$$\therefore \quad V_R = \frac{R_2 V_B + V_{BE}(R_1 - 2R_2)}{R_1 + R_2}$$

Differentiating V_B & V_{BE} partially w.r.t. temperature

$$0 = \frac{R_2}{R_1 + R_2} \frac{\partial V_B}{\partial T} + \left[\frac{(R_1 - 2R_2)}{R_1 + R_2}\right] \frac{\partial V_{BE}}{\partial T}$$

$$\frac{2R_2 - R_1}{R_2} = \frac{\partial V_B / \partial T}{\partial V_{BE} / \partial T}$$

∴ To be satisfied for obtaining zero temperature co-efficient.

Apply KCL at node 'N'

$$\frac{V_B - V_{BE}(Q_1) - V_{BE}(D_1) - V_R}{R_1} = \frac{V_R - V_{BE}(D_2)}{R_2}$$

Assume matched transistors,

$$V_{BE}(Q_1) = V_{BE}(D_1) = V_{BE}(D_2) = V_{BE}$$

Then V_B: $\frac{V_B - 2V_{BE} - V_R}{R_1} = \frac{V_R - V_{BE}}{R_2}$

$$V_R = \frac{R_2 V_B + V_{BE}(R_1 - 2R_2)}{R_1 + R_2}$$

Diff V_B & V_{BE} partially w.r.t temperature

(1.5) BJT DIFFERENTIAL AMPLIFIER WITH ACTIVE LOADS

1.5.1 : Differential amp with active loads.

- Diff Amp are designed with active loads to increase differential mode voltage gain
- Open ckt voltage gain of an op-amp is needed to be as large as possible which is acheived by cascading gain stages which increases phase shift and amp also becomes vulnerable to oscillations.
- Gain is ↑ed by large value of collector resistance

  voltage gain, $A_{dm} = -g_m R_c = -\frac{I_C R_C}{V_T}$ → (1)

- To increase the gain the $I_C R_C$ must be very large.
- Limitations in IC fabrication:
  - → large value of resistance needs a large chip area
  - → for large Rc, quiescent drop across resistor increases and large power supply will be required to maintain operating current.
  - → Large monolithic resistor introduces large parasitic capacitances which limits the frequency response of amplifier.
  - → For linear operation of differential pair, device should not be allowed to enter into saturation.

  For these reasons we prefer active loads in differential amplifier.

1.5.2 BJT differential amplifiers using active loads:

- Simple active load ckt for a differential amp. is current mirror active loads. o
- Active loads comprise of transistors Q_3 & Q_4 with transistor Q_3 connected as a diode with base. collector terminal.
- ckt drives load resistor R_L
- An AC i/p voltage is applied to differential amplifier

Various currents of ckt is

$$I_{C4} = I_{C3} = I_{C1} = \frac{g_m V_{id}}{2} \rightarrow (2)$$

where, $I_{C4} = I_{C3}$ (due to current mirror)

$$I_{C2} = -\frac{g_m V_{id}}{2} \quad \rightarrow (3)$$

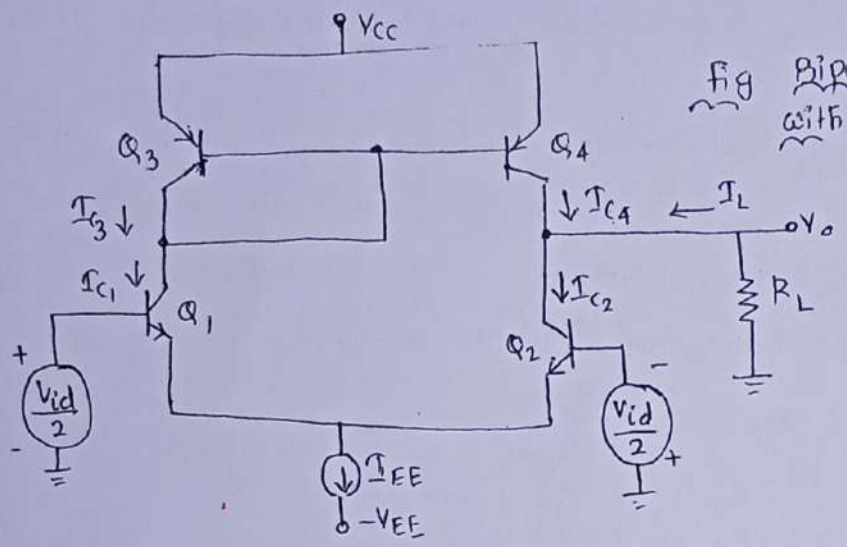


fig Bipolar differential amplifier with current mirror active loads

- Load current I_L entering next stage is,

$$I_L = I_{C2} - I_{C4} \quad \rightarrow (4)$$

$$\therefore I_L = -(g_m V_{id})/2 - (g_m V_{id})/2 = -g_m V_{id} \quad \rightarrow (5)$$

- O/P voltage, $V_o = -I_L R_L \quad \rightarrow (6)$

$$= -(-g_m V_{id}) R_L$$

$$= g_m V_{id} R_L \quad \rightarrow (7)$$

A'C voltage gain of ckt

$$A_V = \frac{V_o}{V_{id}} = \frac{g_m R_L V_{id}}{V_{id}} = g_m R_L \quad \rightarrow (8)$$

- Differential amplifier can amplify differential I/P signals and it provides single-ended o/p with a ground reference. Since R_L is connected to only one o/p terminal
- this is made use of current mirror active loads.
- o/p resistance R_o of ckt offered by parallel combination of Q_2 (NPN) & Q_4 (PNP)

$$\therefore R_o = r_{o2} \| r_{o4} \quad \rightarrow (9)$$

Analysis of BJT differential amplifier with active loads

- Assume, $\frac{V_{id}}{2} = 0$, for Q_1 & Q_2 & $\beta = \infty$
- Bias current is divided equally b/w Q_1 & Q_2

$$\therefore I_{C_1} = I_{C_2} = I_{EE}/2 \longrightarrow (10)$$

- I_{C_1} supplied by Q_3 is mirrored as I_{C_4} at o/p of transistor Q_4.

$\therefore I_{C_3} = I_{C_4} = I_{EE}$ & dc current in collector of Q_4 is exactly the current needed to satisfy Q_2.

- When β is very large, $V_{EC4} = V_{EC3} = V_{BE}$, the current mirror ratio becomes exactly unity.
- Differential amplifier is completely balanced, o/p voltage

$$V_o = V_{CC} - V_{BE} \longrightarrow (11)$$

Q-point :-

- The collector currents of all transistors are equal

$$\text{i.e } I_{C_1} = I_{C_2} = I_{C_3} = I_{C_4} = \frac{I_{EE}}{2} \longrightarrow (12)$$

- Collector-Emitter voltage of Q_1 & Q_2 are given by

$$V_{CE1} = V_{CE2} = V_C - V_E$$

$$= (V_{CC} - V_{EB}) - (-V_{EB}) \simeq V_{CC} \longrightarrow (13)$$

- Collector-Emitter voltage of Q_3 & Q_4

$$V_{CE3} = V_{CE4} = V_{EB} \longrightarrow (14)$$

- I/p offset voltage V_{os} of differential amplifier arise from mismatch in i/p device Q_1 & Q_2, load devices Q_3, Q_4 from base currents of load devices.

$$V_{os} \simeq V_T \left[\frac{\Delta I_{SP}}{I_{SP}} - \frac{\Delta I_{SN}}{I_{SN}} + \frac{2}{\beta} \right] \longrightarrow (15)$$

- where 'β' represents the gain of PNP transistor

$$\Delta I_{SP} = I_{S3} - I_{S4} \longrightarrow (16)$$

$$I_{SP} = \frac{I_{S3} + I_{S4}}{2} \longrightarrow (17)$$

$$\Delta I_{SN} = I_{S1} - I_{S2} \longrightarrow (18)$$

$$I_{SN} = \frac{I_{S1} + I_{S2}}{2} \longrightarrow (19)$$

Assume a worst case value, ± 4% for $\frac{\Delta I_S}{I_S}$ & $\beta = 20$

$$V_{OS} = V_T (0.04 + 0.04 + 0.1)$$

$$= 26 \times 10^{-3} \times 0.18 \simeq 4.68 \text{ mV} \quad — (22)$$

Eqn (22) shows offset is higher than that of a resistive loaded differential amplifier. This is reduced by use of emitter resistors for Q_3 & Q_4 & Q_5 in current mirror load

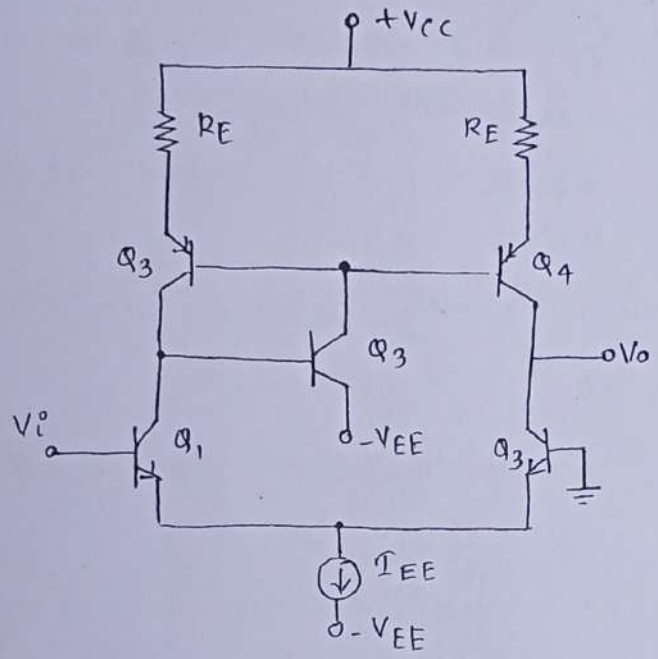
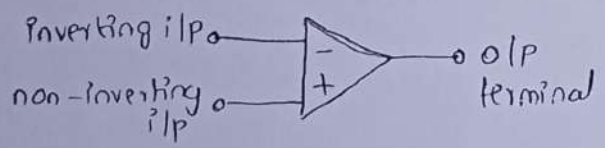


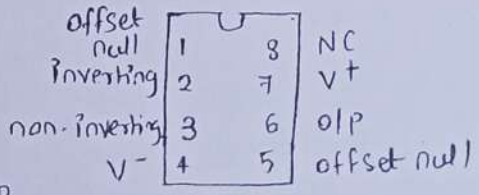
fig. Improved differential ckt using active load

(1.6) BASIC INFORMATION ABOUT OP-AMPS:

Circuit Symbol:

- ckt schematic of an op-amp is a triangle





- It has 2 i/p terminals & one o/p
- Terminal with "-" sign is called "inverting i/p terminal"
- Terminal with '+' sign is called "non-inverting i/p terminal."

Packages: 3 popular packages available

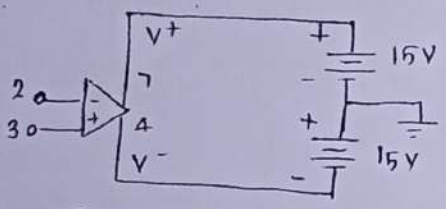
- Metal can (TO) package
- Dual in-line package (DIP)
- Flat package of flat pack

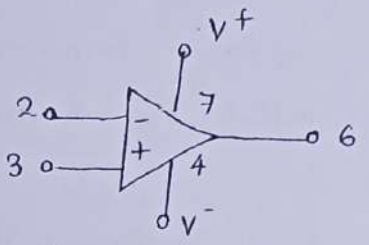
~~o/p~~ Op Amp Terminals:

5 basic terminals: 2 i/p terminals
1 o/p terminal
2 power supply terminal

Power Supply Connections:

- V^+ & V^- power supply terminals connected to 2 dc voltage source
- V^+ → connected to positive terminal of one source
- V^- pin → " " negative "



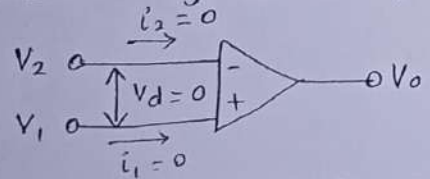


Power Supply range: ±5V to ±22V

- Common point of 2 supplies must be grounded, twice supply voltage will get applied & damage the op-amp

(1.7) IDEAL OPERATIONAL AMPLIFIER:-

- Schematic symbol of op-amp



- It has 2 i/p terminals & one o/p terminal
- '−' & '+' refers to inverting & non-inverting i/p terminal

i.e $V_1 = 0$, $V_o = 180°$ out of phase with i/p V_2

$V_2 = 0$, V_o = inphase with i/p V_1

- Op-amp is said to be ideal if it has following characteristics

→ open loop voltage gain, $A_{OL} = \infty$
→ I/p impedance, $R_i = \infty$
→ o/p impedance, $R_o = 0$
→ Bandwidth $BW = \infty$
→ zero offset, $V_o = 0$, when $V_1 = V_2 = 0$

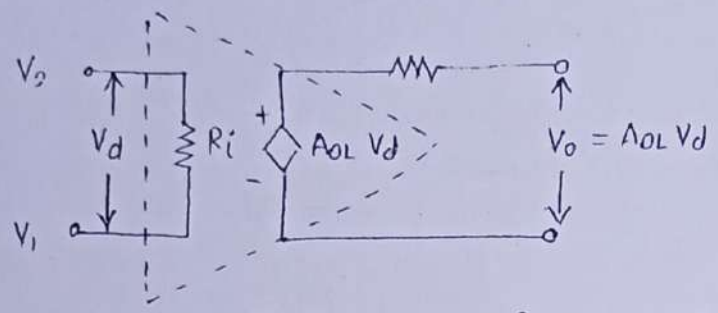


fig. Equivalent ckt of an Op Amp

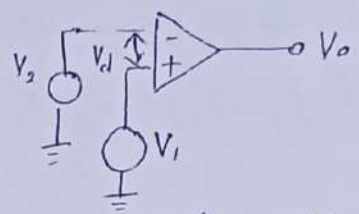


fig. open loop ckt

- An ideal Op-amp draws no current at both i/p terminals i.e. $\boxed{I_1 = I_2 = 0}$ (∵ infinite i/p impedance)
- Since gain is ∞, voltage between inverting & non-inverting terminals i.e. differential i/p voltage $\boxed{V_d = V_1 - V_2}$ is zero for finite o/p voltage V_o
- The o/p voltage V_o is independent of current drawn from o/p as $R_o = 0$.

But these op-amp can't be realized in practice

From equivalent ckt, $A_{OL} \neq \infty$, $R_i \neq \infty$, $R_o \neq 0$

∴ Op-amp is voltage controlled voltage source, A_{OL} & V_d are equivalent. Thevenin voltage source & R_o is Thevenin's equivalent resistance looking back into o/p terminal

∴ o/p voltage, $V_o = A_{OL} V_d$

$= A_{OL} (V_1 - V_2)$

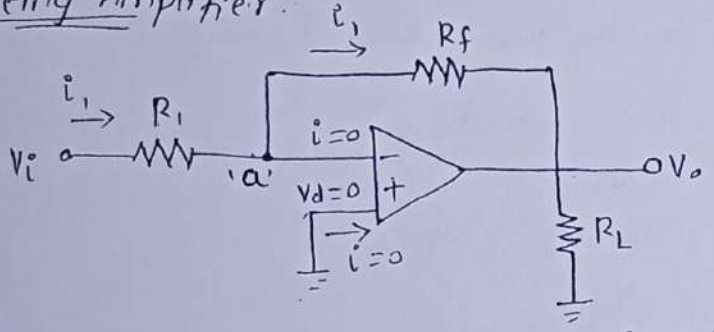
Open loop operation of Op-Amp.

- The simplest way to use op-amp is in open loop model
- V_1 & V_2 are applied at non-inverting & inverting terminal Since gain is infinite. $V_o = +V_{sat}$ or $-V_{sat}$ as $V_1 > V_2$ or $V_2 > V_1$
- o/p assumes one of 2 possible states $+V_{sat}$ / $-V_{sat}$ & amplifier act as switch

Feedback in Ideal Op-Amp.:

- Utility is improved by providing negative feedback. O/P is not driven into saturation & ckt behaves in linear manner
- Two important negative feedback circuits are
  (a) current drawn by either of the i/p terminals (inverting / non-inverting) is negligible
  (b) The differential i/p voltage V_d b/w non-inverting & inverting i/p terminals is zero

Inverting Amplifier:



- O/P voltage V_o is fed back to inverting i/p terminal through $R_f = R_1$ n/w where R_f is feedback resistor
- I/P signal V_i (AC/DC) is applied to inverting i/p terminal through R_1 & non-inverting terminal is grounded

Analysis: Assume ideal op-amp

$V_d = 0$, at node 'a' which is at ground potential & current i_1 through R_i is $\boxed{i_1 = V_i/R_i}$ → (1)

- Op-amp draws no current, all current flowing through R_1 must flow through R_f $\quad V_o = IR$

$$\Rightarrow V_o = -i_1 R_f = -V_i \frac{R_f}{R_1} \quad \rightarrow (2)$$

Gain of inverting amplifier,

$$A_{CL} = \frac{V_o}{V_i} = -\frac{R_f}{R_1}$$

Nodal equation at node 'a': $\frac{V_a - V_i}{R_1} = -\frac{(V_a - V_o)}{R_1}$

$$\frac{V_a - V_i}{R_1} + \frac{V_a - V_o}{R_f} = 0$$

Output stage is designed to provide low output impedance
output voltage should swing symmetrically with respect to ground
Power supply ± 15 V.

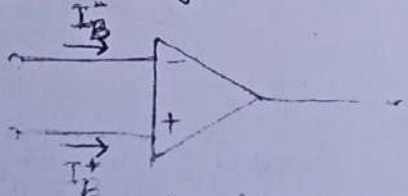
DC CHARACTERISTICS :-

* Ideal op-amp draws no current from source and also independent of temperature.
* But in practical op-amp current is drawn and two inputs responds differently to current and voltage due to mismatch in transistors. & temperature : is dependent shifts in operation.

  ↳ Input bias current
  ↳ Input offset current
  ↳ Input offset voltage
  ↳ Thermal drift.

↳ INPUT BIAS CORRENT :-

* Op-amp input is differential amplifier made of BJT/FET.
* Input transistors must be biased into their linear region by supplying current into bases by external circuit.
* In ideal op-amp, Assumption: no current is drawn from input terminal.
* Practically, input terminal conduct small value of dc current to bias the input transistors.
* Base current entering inverting & non-inverting terminal I_B^- & I_B^+



* Even though both transistors are identical, $I_B^- \neq I_B^+$ due to internal imbalance between two inputs

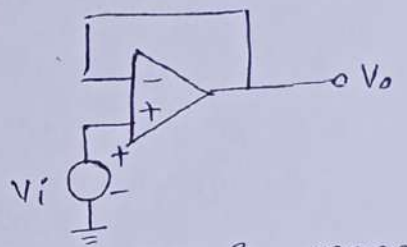
∴ For non-inverting amplifier the voltage gain

$$A_{CL} = \frac{V_o}{V_i} = 1 + \frac{R_f}{R_1}$$

- The gain can be adjusted to unity / more by proper selection of resistor R_f and R_1
- Compared to inverting amplifier, input resistance of non-inverting amplifier is large.

Voltage follower:

- In non-inverting amplifier if $R_f = 0$ & $R_1 = \infty$, we get following fig. i.e voltage follower



$$A_{CL} = \frac{V_o}{V_i}$$

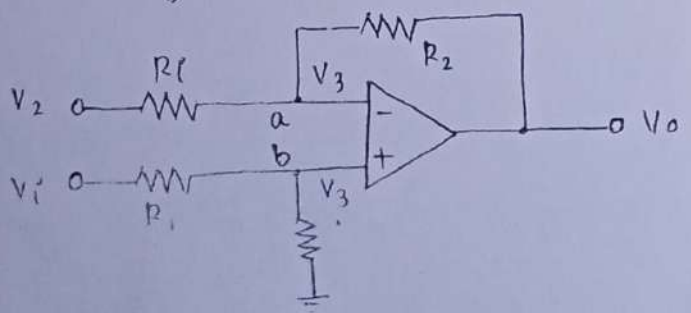
$$V_o = V_i$$

i.e o/p voltage is equal to i/p voltage both in magnitude and phase, i.e o/p voltage follower i/p voltage exactly so ckt is called voltage follower.

- Use of unity gain ckt beroz of i/p impedance is very high in MΩ & o/p impedance is zero. So it draw negligible current.
- So voltage follower is used as buffer for impedance matching connect high impedance to low impedance

Differential Amplifier:

- ckt that amplifies the difference b/w two signals is called a difference / differential amplifier
- It is very useful in instrumentation ckt



where 'Va' is voltage at node 'a' node 'a' is at virtual ground $\boxed{V_a = 0} \Rightarrow \frac{-V_i}{R_1} + \left[\frac{-V_o}{R_f}\right] = 0 \;\Big\|\; \frac{-V_i}{R_1} = \frac{V_o}{R_f}$

$$\therefore A_{CL} = \frac{V_o}{V_i} = -\frac{R_f}{R_1}$$

'–' Sign indicate a phase shift of 180° b/w V_i and V_o

$R_1 \rightarrow$ effective i/p impedance (∵ Inv i/p termind is at virtual ground)

→ large value to avoid loading effect

→ limits gain that can be obtained from this ckt

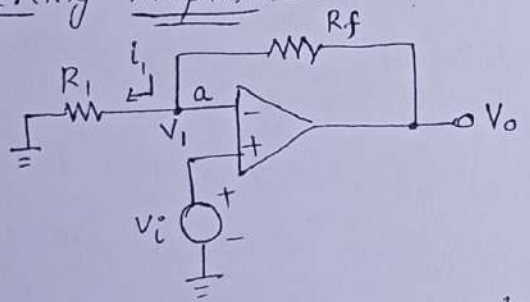
R_L (load resistor)

↳ at o/p otherwise the i/p impedance of the measuring device such as oscilloscope

$R_1 \rightarrow Z_1$ & $R_f \rightarrow Z_f$

∴ voltage gain, $A_{CL} = \frac{-Z_f}{Z_i}$

Non-Inverting Amplifier:



- If signal is applied to non-inverting i/p terminal & feedback is given, ckt amplifies without inverting the i/p signal so ckt is called non-inverting amplifier
- Negative feedback s/m as o/p is fed back to inverting i/p
- Differential voltage V_d at i/p of op-amp is zero & voltage at 'a' is V_i
- R_f & R_i forms a potential divider

$$V_i = \frac{V_o}{R_1 + R_f} R_1$$

No current flows into op-amp

$$\frac{V_o}{V_i} = \frac{R_1 + R_f}{R_1} \quad \text{or} \quad 1 + \frac{R_f}{R_1}$$

• At i/p terminal - differential voltage of op-amp is zero, node 'a' & 'b' are at same potential "V_3"

Nodal eqn at "a" : $\frac{V_3 - V_2}{R_1} + \frac{V_3 - V_o}{R_2} = 0$ → ①

At node "b" : $\frac{V_3 - V_1}{R_1} + \frac{V_3}{R_2} = 0$ → ②

Rearranging ① $\frac{V_3}{R_1} - \frac{V_2}{R_1} + \frac{V_3}{R_2} - \frac{V_o}{R_2} = 0$

$$V_3\left[\frac{1}{R_1} + \frac{1}{R_2}\right] - \frac{V_2}{R_1} = \frac{V_o}{R_2} \quad \rightarrow ③$$

Rearranging ②, $\frac{V_3}{R_1} - \frac{V_1}{R_1} + \frac{V_3}{R_2} = 0$

$$\left[\frac{1}{R_1} + \frac{1}{R_2}\right]V_3 - \frac{V_1}{R_1} = 0 \quad \rightarrow ④$$

Subtract ④ from ③

$$\Rightarrow \left[\frac{1}{R_1} + \frac{1}{R_2}\right]V_3 - \frac{V_2}{R_1} - \left[\frac{1}{R_1} + \frac{1}{R_2}\right]V_3 + \frac{V_1}{R_1} = 0 - 0$$

$$\Rightarrow \frac{1}{R_1}(V_1 - V_2) = \frac{V_o}{R_2} \quad \rightarrow ⑤$$

$$\boxed{V_o = \frac{R_2}{R_1}(V_1 - V_2)} \quad \rightarrow ⑥$$

• ckt is very useful in detecting very small difference in signals & gain R_2/R_1 is chosen very large.

1.8 General Operational Amplifier Stages

Consists of 4 stages

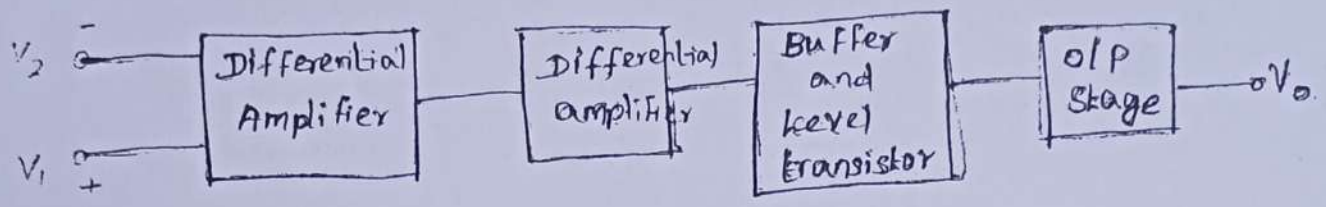


fig: Block Schematic of OP-AMP

- First 2 stages are cascaded differential amplifiers used to provide high gain & high i/p resistance
- Third stage act as buffer as well as level shifter
- Buffer is usually emitter follower whose i/p impedance is very high to prevent loading of high gain stage
- Level shifter will adjust dc voltages so $V_o = 0$, when $V_i = 0$
- o/p stage is designed to provide low o/p impedance, o/p voltage should swing symmetrically with respect to ground
- Power Supply = ± 15 V

Operational Amplifier internal ckt

(a) Differential amplifier:

- Main purpose is to provide high gain to difference-mode signal, Cancel the common-mode signal
- Relative sensitivity of an op-amp to a difference sgnl as compared to common-mode signal is called "CMRR"
- High the value of CMMR, better is the op-amp
- Cascaded direct coupled amp. can provide high gain down to zero freq as it has no coupling capacitor
- However it suffers from drift due to temperature dependency of I_{CO}, V_{BE}, h_{FE} of transistor, which can be eliminated by using balanced or differential amplifier as shown

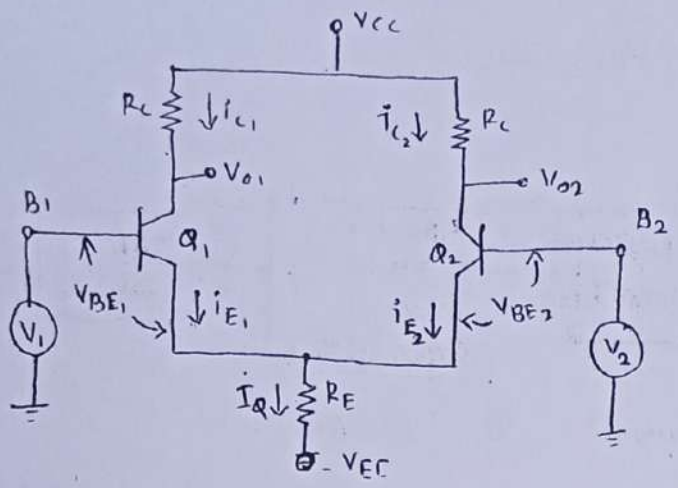


Fig. Basic differential amplifier

The 4 configuration of differential amp. are

(i) Differential - i/p, differential - o/p (or) dual - i/p balanced o/p

(ii) Differential - i/p single ended - o/p

(iii) Single i/p, differential o/p

(iv) Single - i/p, single ended - o/p

→ If sgnl applied at both i/p, it is differential i/p (or) dual

→ If o/p is measured b/w collectors, it is differential o/p

(b) Transfer characteristics:

The collector current i_{C_1} & i_{C_2} for Q_1 & Q_2 are

$$i_{C_1} = \alpha_F I_{ES} \, e^{V_{BE_1}/V_T} \quad \rightarrow (1)$$

$$i_{C_2} = \alpha_F I_{ES} \, e^{V_{BE_2}/V_T} \quad \rightarrow (2)$$

From (1) & (2), $\frac{i_{C_1}}{i_{C_2}} = e^{(V_{BE_1} - V_{BE_2})/V_T} \quad \rightarrow (3)$

Apply KVL, for loop has 2 emitter - base jn.

$$V_1 - V_{BE_1} + V_{BE_2} - V_2 = 0$$

(or) $$V_{BE_1} - V_{BE_2} = V_1 - V_2 = V_d$$

where, 'V_d' is diff. of 2 i/p voltage

It is observed that

(i) For $V_d > 4 V_T$, $i_{C_1} = \alpha_F I_Q$, $i_{C_2} = 0$

Hence, $V_{o1} = V_{cc} - \alpha_F I_Q R_c$

$V_{o2} = V_{cc}$

(2) For $V_d < -4 V_T$, $i_{c1} = 0$, $i_{c2} = \alpha_F I_Q$

Hence $V_{o1} = V_{cc}$, V_{o2} is negligible

(3) Differential amp function as a very good limiter

(4) It can also fn as automatic gain ctrl

(5) B/w value $-2V_T \leq V_d \leq 2V_T$, it functions as linear amp.

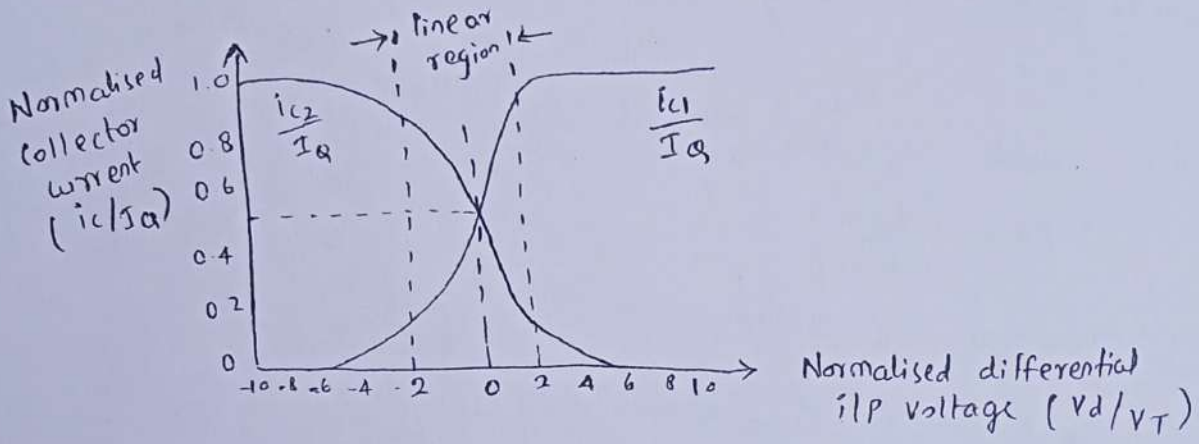
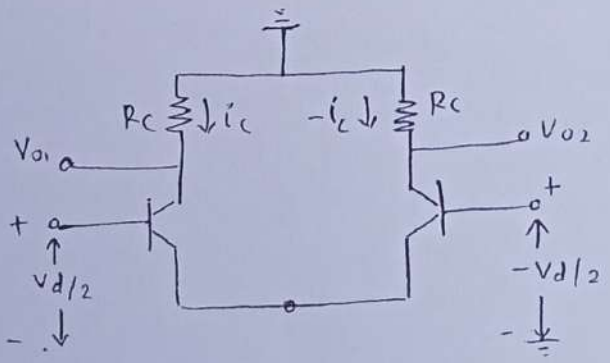


fig. Transfer characteristics of Diff Amp

(C) Low frequency Small signal analysis:

- An ideal dual-i/p balanced-o/p differential amplifier is



- It amplifies only differential sgnl at 2 i/p
- Rejects signal common to these i/p
- Any unwanted signal such as noise, would be rejected

The a.c analysis can be performed either by hybrid π model, or h-parameter model

→ Differential mode gain, A_{DM}

(i) using hybrid π - model, $A_{DM} = \frac{V_{o1} - V_{o2}}{V_d} = -g_m R_c$

(ii) using h- parameter, $A_{DM} = \frac{V_{o1} - V_{o2}}{V_d} = -\frac{h_{fe} R_c}{h_{ie}}$

→ Common-mode gain, A_{CM} using h- parameter

$$A_{CM} = \frac{V_{o1}}{V_{o2}} = \frac{-h_{fe} R_c}{h_{ie} + (1+h_{fe}) 2R_E}$$

The common-mode rejection ratio (CMRR)

$$CMRR = \left| \frac{A_{DM}}{A_{CM}} \right|$$

(d) Circuits for improving CMRR :-

- For CMRR to be large, A_{CM} should be less
- With current constant, the ~~CMRR~~ A_{CM} is zero
- Small signal current flowing through load resistor is zero resulting zero o/p voltage
- IC op-amp μA 741 uses a constant current source which very simple & use less number of current circuit is known as current mirror
- It offers large resistance under any circumstances, thereby high value of CMRR

$$I_B = \frac{I_B^+ + I_B^-}{2}$$

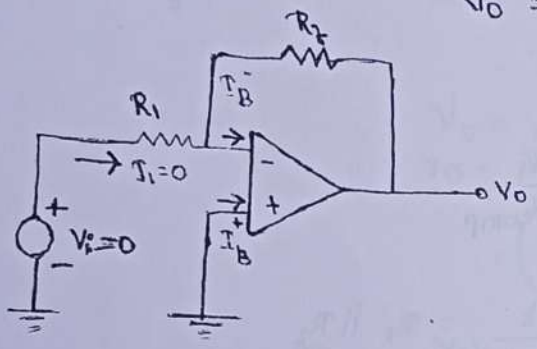
* For 741, bipolar op amp, bias current is 500nA or less.
  FET input opamp, bias current as low as 50pA at room temperature

* Consider, basic inverting amplifier, $V_i = 0V$ & $V_o = 0V$ but output voltage is offset by,

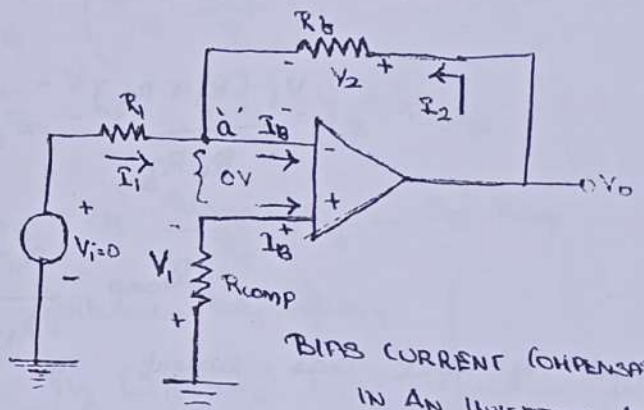
$$V_o = (I_B^-) R_f$$

For a 741 op amp with $1M\Omega = R_f$

$$V_o = 500\,nA \times 1M\Omega = 500mV.$$



INVERTING AMPLIFIER WITH BIAS CURRENT



BIAS CURRENT COMPENSATION IN AN INVERTING AMPLIFIER

* Signal level is measured in millivolts, that is unacceptable, this compensated by R_{comp} added between non inv input terminal and ground.
* current I_B^+ flowing through R_{comp} develops a voltage V_1 across it.

By KVL,

$$-V_1 + 0 + V_2 - V_o = 0$$

$$V_o = V_2 - V_1$$

* By properly selecting value of R_{comp}, V_2 can be cancelled with V_1 & $V_o = 0$

R_{comp} derived

$$V_1 = I_B^+ R_{comp}$$

$$I_B^+ = \frac{V_1}{R_{comp}}$$

* Node 'a' is at voltage $(-V_1)$ because of non-inverting input terminal $(-V_1)$

$V_i = 0$; we get $I_1 = \frac{V_1}{R_1}$

$$I_2 = V_2$$

* For compensation, V_o should be zero. for $V_i = 0$.

From $V_o = V_2 - V_1$

$$V_2 = V_1.$$

So that $$I_2 = \frac{V_1}{R_2}$$

KCL at node 'a' gives

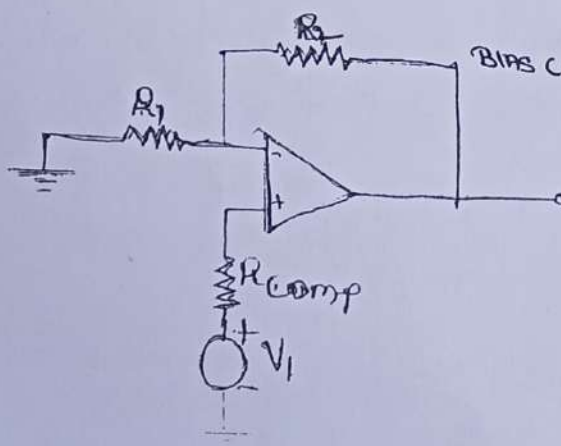
$$I_B^- = I_2 + I_1 = \frac{V_1}{R_2} + \frac{V_1}{R_1} = V_1 \frac{(R_1 + R_2)}{R_1 R_2}.$$

Assuming $I_B^- = I_B^+$.

$$\frac{V_1 (R_1 + R_2)}{R_1 R_2} = \frac{V_1}{R_{comp}}$$

$$R_{comp} = \frac{R_1 R_2}{R_1 + R_2} = R_1 \,||\, R_2.$$

* Effect of input bias current in non-inverting amplifier, compensated by placing R_{comp} in series with V_1



BIAS CURRENT COMPENSATION IN A NON-INVERTING AMPLIFIER.

↳ INPUT OFFSET CURRENT :

* The bias current compensation will work only when $I_B^+ = I_B^-$ Since o/p transistors cannot made identical, $I_B^+ \neq I_B^-$ This difference is called offset current I_{os}

$$|I_{os}| = I_B^+ - I_B^-$$

| ↳ indicates we can not predict I_B^+ or I_B^- will be higher.

I_{os} ⇒ BJT op amp = 200nA

FET op amp = 10pA

* I_{os} produce o/p voltage, even when $V_i = 0$

$$V_1 = I_B^+ R_{comp}$$

$$I_1 = \frac{V_1}{R_1}$$

KCL at node 'a' gives,

$$I_{2)} = (I_B^- - I_1)$$

$$= I_B^- - \left(I_B^+ \frac{R_{comp}}{R_1}\right)$$

$$V_o = V_2 - V_1$$

$$V_O = I_a R_f - V_1 = I_a R_f - I_B^+ R_{comp}$$

$$= \left(I_B^- - I_B^+ \frac{R_{comp}}{R_1}\right) R_f - I_B^+ R_{comp}$$

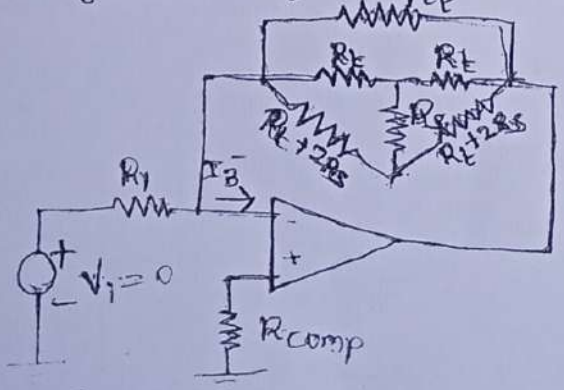
Sub R_{comp} value & algebraic Manipulation,

$$V_O = R_f [I_B^- - I_B^+]$$

$$V_O = R_f I_{os}.$$

* Effect of I_{os} is minimized by keeping R_f small, but R_1 must be kept large but R_f should also maintained high to obtain high gain.

* T- feedback network is used to keep resistance low and also provides feedback signal by T to TI conversion.



INVERTING AMPLIFIER WITH T- FEEDBACK NETWORK.

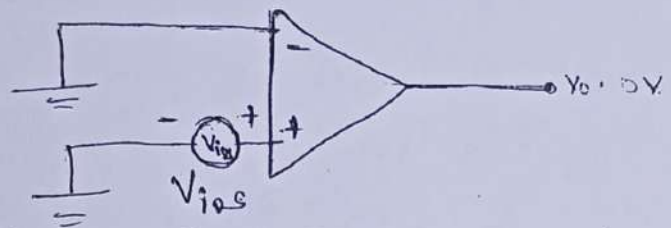
$$R_f \quad \frac{R_t^2 + 2R_t R_s}{R_3}$$

To design, $R_t \ll R_f/20$ then $R_s = \frac{R_t^2}{R_f - 2R_t}$

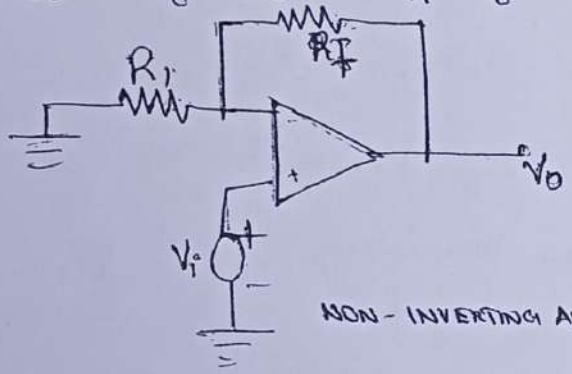
⇒ Input Offset Voltage:

* Output voltage will not be equal to 0 input voltage due to imbalance inside op-amp so small voltage is applied at input to get $V_o = 0$ This voltage is called input offset voltage V_{ios}

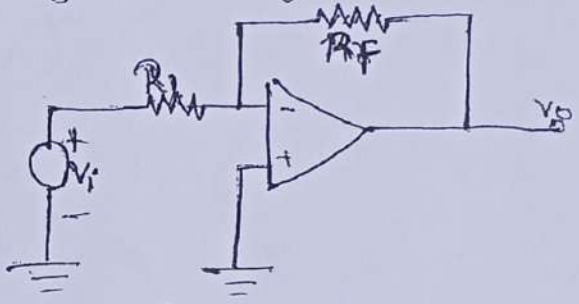
OP AMP SHOWING INPUT OFFSET VOLTAGE



* Effect of V_{ios} on o/p of non-inverting, inverting op-amp is



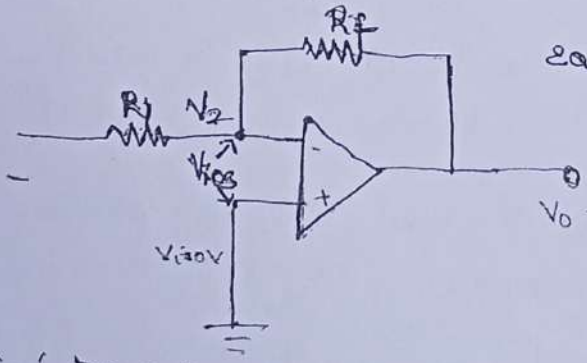
NON-INVERTING AMPLIFIER



INVERTING AMPLIFIER

* If $V_i = 0$, then above two figure become the same.

EQUIVALENT CIRCUIT FOR $V_i = 0$



$$V_o = \left(1 + \frac{R_f}{R_1}\right) V_{ios}$$

* Voltage V_2 at '−' terminal is,

$$V_2 = \left(\frac{R_1}{R_1 + R_2}\right) V_o$$

$$V_o = \left(\frac{R_1 + R_2}{R_1}\right) V_2 = \left(1 + \frac{R_2}{R_1}\right) V_2$$

$$V_{ios} = |V_i - V_2| \text{ and } V_i = 0$$

$$= |0 - V_2| = V_2$$

$$V_o = \left(1 + R_f/R_1\right) V_{ios}$$

Total Output Offset Voltage:

* Total Output offset V_{OT} could be either more or less than the offset voltage produced at the output due to input bias current / input offset voltage alone (bcoz of Vios & I_B either + 've -ve w.r.t ground).

∴ Maximum offset voltage without compensation is

$$V_{OT} = \left(1 + \frac{R_f}{R_1}\right) V_{ios} + R_f I_B$$

* With Rcomp, total o/p offset voltage,

$$V_{OT} = \left(1 + \frac{R_f}{R_1}\right) V_{ios} + R_f I_\alpha$$

Thermal Drift

* Bias current, offset current and offset voltage change with temperature.

* A circuit carefully nulled at 25°C may not remain so when the temperature rises to 35°C. This is called drift.

* offset current drift = nA/°C
  offset voltage drift = mV/°C

* Techniques to minimize effect of drift:
  - Careful printed circuit board layout used to op-amp away from source of heat.
  - Forced air cooling may be used to stabilize the ambient temperature.

AC CHARACTERISTICS :-

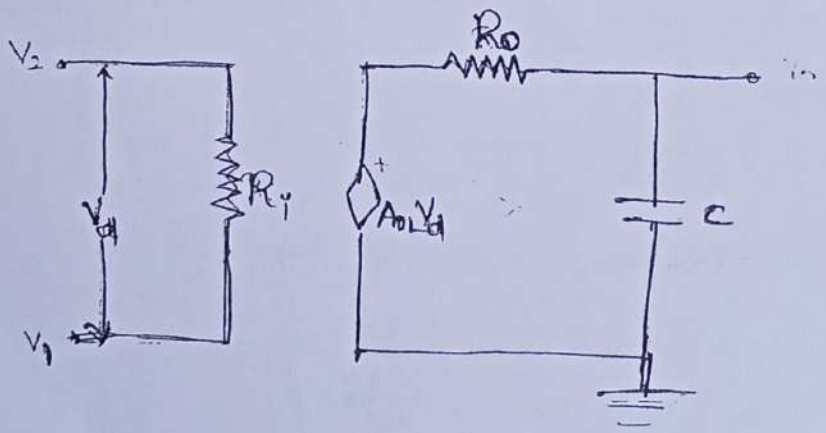
* For small signal sinusoidal (AC) applications,
  - ↳ Frequency Response
  - ↳ Slew - rate.

↳ Frequency Response

* Ideal op-amp have infinite bandwidth open loop gain is 90 db with dc signal its gain should remain the same through audio / high radio frequency.
* Practical op amp gain, however, decreases at high frequencies.

Gain of op-amp to roll off after certain frequency

* Bcoz of capacitive component in Equivalent ckt → capacitance
* Physical characteristics of device (BJT / FET)
* Op amp with only one break (corner) frequency ⇒ capacitor effect represents by single capacitor C.



HIGH FREQUENCY MODEL OF AN OP-AMP WITH CORNER FREQUENCY (F_1)

* High frequency is a modified version of low frequency model with capacitor C at output ⇒ one pole due to R_oC 2 decibels/decade roll off

1.10 AC PERFORMANCE CHARACTERISTICS:

DC characteristics affect the steady state (dc) response of op amp only. For small sinusoidal (ac) applications, one has to know the ac characteristics such as frequency response & slew-rate.

1.10.1 Frequency response:

- Ideal op-amp have infinite bandwidth, Open loop gain is 90dB with dc signal. Its gain should be the same through audio & Radio frequency.
- In practical op amp, however gain decreases at high frequencies Thus gain of op amp roll-off after certain frequencies.
- Because of the capacitive component in equivalent ckt, which is caused by physical characteristics of device (BJT/FET)
- Op-amp has one break (corner) frequency → capacitor effect represents by single capacitor C.

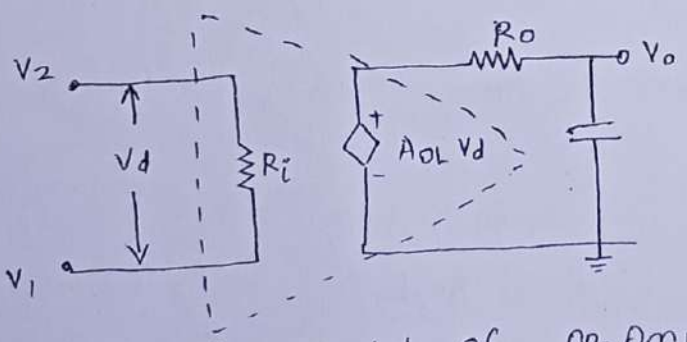


fig. High freq. model of op-Amp with single corner freq.

- High freq is a modified version of low freq model with capacitor 'C' at O/P There is one pole due to Rc is -20dB/decade roll off

Open loop voltage gain, $V_o = \frac{-jX_C}{R_o - jX_C} A_{OL} V_d$

$$A = \frac{V_o}{V_i} = \frac{A_{OL}}{1 + j 2\pi f R_o C}$$

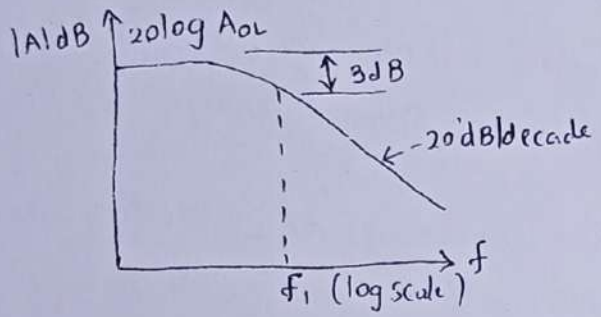
$$= \frac{A_{OL}}{1 + j(f/f_1)}$$

where $f_1 = \frac{1}{2\pi R_o C}$ ⇒ corner freq or upper 3-dB freq of op-amp

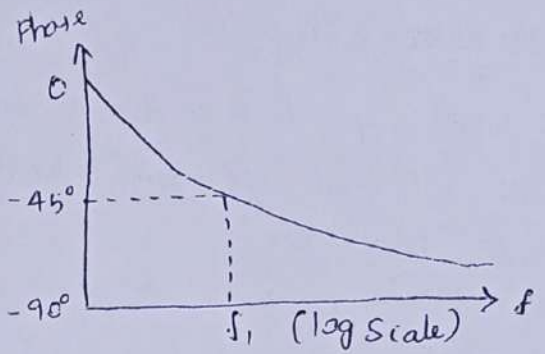
Magnitude, $|A| = \frac{A_{OL}}{\sqrt{1+(f/f_1)^2}}$

phase angle $\phi = -\tan^{-1}(f/f_1)$

Magnitude & phase characteristics



Fig(a) open loop magnitude characteristics in semilog paper



fig(b): phase characteristics for an op-amp with single break frequency

(i) for $f < f_1$, $|A|$ of gain is $20\log A_{OL}$ in dB

(ii) At $f = f_1$, gain is 3dB down from dc value of A_{OL} in dB
'f_1' is corner freq

(iii) $f >> f_1$, gain rolls-off at the rate of -20dB/decade or -6dB/octave

Phase characteristics: At $f = 0$, phase angle $= 0°$

At corner freq f_1, phase angle is $-45°$ (lagging)

At infinite freq., phase angle is $-90°$

∴ Maximum of 90° phase change occurs with single capacitor

• for practical purpose, zero freq = 1 decade below f_1

infinite freq = 1 decade above f_1

Voltage Transfer function in S-domain

$$A = \frac{A_{OL}}{1+j(f/f_1)} = \frac{A_{OL}}{1+j(\frac{\omega}{\omega_1})} = \frac{A_{OL}}{\frac{\omega_1+j\omega}{\omega_1}}$$

$$= \frac{A_{OL}\,\omega_1}{\omega_1+j\omega} = \frac{A_{OL}\,\omega_1}{S+\omega_1} \quad (\because S = j\omega)$$

- A practical op amp has number of stages, each stage produce capacitive component, due to no of RC pole pairs, there will be number of break frequencies.

∴ Transfer function of op amp with 3 break frequencies

$$A = \frac{A_{OL}}{\left(1+j\frac{f}{f_1}\right)\left(1+j\,f/f_2\right)\left(1+j\,f/f_3\right)} \quad ; \quad 0 < f_1 < f_2 < f_3$$

$$= \frac{A_{OL}}{\left(\frac{\omega_1+j\omega}{\omega_1}\right)\left(\frac{\omega_2+j\omega}{\omega_2}\right)\left(\frac{\omega_3+j\omega}{\omega_3}\right)}$$

$$= \frac{A_{OL}\cdot\omega_1\cdot\omega_2\cdot\omega_3}{(s+\omega_1)(s+\omega_2)(s+\omega_3)} \quad ; \text{ with } 0 < \omega_1 < \omega_2 < \omega_3$$

- For the below figure, as frequency increases, cascading effect of RC pairs comes into effect. Roll-off rate increases successively by -20dB/decade at each corner frequency.
- Each RC pole pair introduce lagging phase of maximum upto -90°.

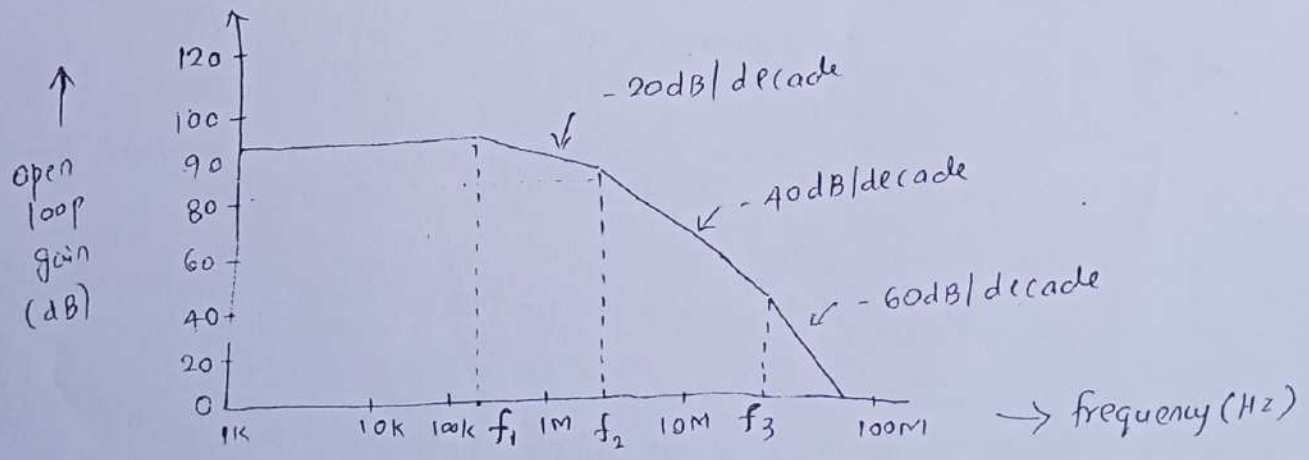


Fig Approximation of open loop gain vs frequency curve

1.10.2 Stability of an Op-Amp:

- Op amps are rarely used in open loop configuration because of high gain
- Consider effect of feedback on freq. response

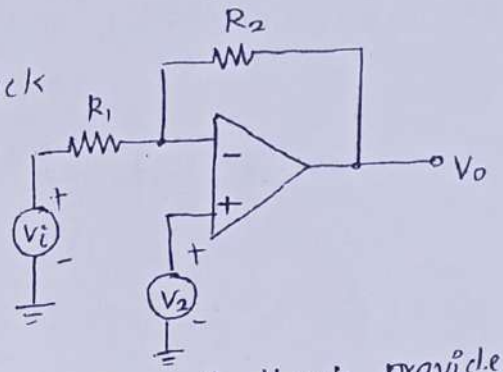
Op-amp use resistive feedback n/w, $V_2 = 0$ for inverting amp & $V_1 = 0$ for non-inv amplifier

closed loop transfer fn : -ve feedback

$$\boxed{A_{CL} = \frac{A}{1+A\beta}} \rightarrow (1)$$

where, A = open loop voltage gain

β = feedback ratio



Resistive feedback provided in Op-Amp

From (1),

characteristic eqn $(1+A\beta) = 0$

Thus ckt becomes unstable, leads to sustained oscillation

Rewriting, $1-(-A\beta) = 0$ leads to, loop gain : $-A\beta = 1 \rightarrow (2)$

$A\beta$ = Complex quantity, $|A\beta| = 1$

Phase condition : $\angle -A\beta = 0$ (or multiple of 2π)

$\angle A\beta = \pi$ (or multiple of π)

- In the ckt, feedback n/w is resistive n/w and it doesn't provide any phase shift ∴ op-amp is in inverting mode, provide 180° phase shift at low freq.
- At high freq., additional -90° phase shift occurs in open loop gain due to corner frequency.
- Two corner frequencies, maximum of phase shift associated with gain A is -180°
- At high freq., some value of β, magnitude of $A\beta$ = unity, when A has additional phase shift of 180°, which makes total phase shift = 0
- Amplifier begin to oscillate as both magnitude & phase condition laid down, oscillation is just the starting point of instability

Instability -> unbounded o/p

$(1+A\beta) < 1$

$A\beta < 0$ i.e negative

→ Then $A_{CL} > A$, i.e closed loop gain increases & leads instability
→ phase contribution = zero

- At low frequency, additional phase contribution of A is zero,

$A\beta > 0$, $A_{CL} < A$, s/m is stable

- At high frequency, s/m 'A' have 3 corner freq. or 3 RC pole pair, Possible of open loop gain A to contribute a maximum of $-270°$ phase shift

$\therefore A\beta = -ve$, instability occurs

- For stable operation, the rate of closure b/w closed loop gain and open-loop curve should not exceed -20 dB/decade.
- At high freq., for lower closed loop gain, the feedback become significant & regenerative. It create sustained oscillation

For Quantitative discussion about stability,

Transfer fn., of op-amp characterized by 3 poles

$$A = \frac{-A_{OL}\,\omega_1\omega_2\omega_3}{(s+\omega_1)(s+\omega_2)(s+\omega_3)}, \quad 0 < \omega_1 < \omega_2 < \omega_3 \quad \rightarrow (3)$$

Poles of open loop Transfer fn are $-\omega_1, -\omega_2, -\omega_3$

- closed loop poles are P_{CL} that is given by the root characteristic eqn. (from freq. response)

$$1 + A\beta = 0$$

$$\Rightarrow A = \frac{A_{OL}\,\omega_1\omega_2\omega_3}{(s+\omega_1)(s+\omega_2)(s+\omega_3)}$$

Sub 'A' in above eqn

$$\Rightarrow 1 + \frac{\beta A_{OL}\,\omega_1\omega_2\omega_3}{(s+\omega_1)(s+\omega_2)(s+\omega_3)} = 0$$

$$\Rightarrow (s+\omega_1)(s+\omega_2)(s+\omega_3) + \beta A_{OL}\,\omega_1\omega_2\omega_3 = 0 \quad \rightarrow (4)$$

$$(or)\ s^3 + s^2(\omega_1+\omega_2+\omega_3) + s(\omega_1\omega_2 + \omega_1\omega_3 + \omega_2\omega_3) + \omega_1\omega_2\omega_3 + \beta A_{OL}\,\omega_1\omega_2\omega_3 \Big\} = 0$$

$$\Rightarrow s^3 + s^2(\omega_1+\omega_2+\omega_3) + s(\omega_1\omega_2 + \omega_1\omega_3 + \omega_3\omega_3) + \omega_1\omega_2\omega_3\,(1+\beta A_{OL}) \Big\} = 0 \quad \rightarrow (5)$$

Roots of cubic eqn., depends on βA_{OL}, dc loop gain

- $\beta A_{OL} = 0$, roots at $-\omega_1, -\omega_2, -\omega_3$ lie at -ve real axis.
- For small value of βA_{OL}, roots lie on left half of S-plane with one real root, 2 complex conjugate roots (a,a)
- Critical value of βA_{OL} makes System unstable

$$\boxed{a_3 s^3 + a_2 s^2 + a_1 s + a_0 = 0} \quad \rightarrow (6)$$

Comparing (5) & (6)

$$a_3 = 1 \;;\; a_2 = \omega_1+\omega_2+\omega_3 \;;\; a_1 = \omega_1\omega_2 + \omega_1\omega_3 + \omega_2\omega_3 \quad \rightarrow (7)$$
$$a_0 = \omega_1\omega_2\omega_3\,(1+\beta A_{OL})$$

Apply Routh's stability criterion,

(i) All co-efficient of a_3, a_2, a_1 & a_0 should be positive

(ii) $a_1 a_2 - a_3 a_0 = 0$

Sub $\boxed{s = j\omega}$ in (6) $\Rightarrow a_3(j\omega)^3 + a_2(j\omega)^2 + a_1(j\omega) + a_0 = 0$ $= 0$

$\Rightarrow a_3(-j\omega^3) + a_2(-\omega^2) + a_1(j\omega) + a_0$ $= 0$

$\Rightarrow (a_0 - a_2\omega^2) + j\omega(a_1 - a_3\omega^2)$

Real & imaginary parts are equal to zero

$a_0 - a_2\omega^2 = 0$ $\quad\Big|\quad$ $a_1 - a_3\omega^2 = 0$

$\therefore \omega_{osc} = \pm\sqrt{\frac{a_0}{a_2}}$ $\quad\Big|\quad$ $\omega_{osc} = \pm\sqrt{a_1/a_3}$

Sub a_0, a_1, a_2, a_3 from (7)

$\Rightarrow \omega_{osc} = \sqrt{a_1/a_3} = \sqrt{\omega_1\omega_2 + \omega_1\omega_3 + \omega_2\omega_3}$

$\Rightarrow a_0 = \frac{a_1 a_2}{a_3}$ from Routh criteria (ii) $\rightarrow (8)$

$$\Rightarrow \omega_1\omega_2\omega_3\left[1+(\beta A_{OL})_c\right] = \frac{(\omega_1\omega_2+\omega_1\omega_3+\omega_2\omega_3)(\omega_1+\omega_2+\omega_3)}{1}$$

$$\text{(or)} \quad (\beta A_{OL})_c = 2+\frac{\omega_1}{\omega_2}+\frac{\omega_1}{\omega_3}+\frac{\omega_2}{\omega_1}+\frac{\omega_2}{\omega_3}+\frac{\omega_3}{\omega_1}+\frac{\omega_3}{\omega_2} \rightarrow (5)$$

If it is desired that amplifier should remain stable, then A_{OL} must satisfy the condition, $\boxed{\beta = 1}$.

$$\text{i.e} \quad A_{OL} < 2+\frac{\omega_1}{\omega_2}+\frac{\omega_1}{\omega_3}+\frac{\omega_2}{\omega_1}+\frac{\omega_2}{\omega_3}+\frac{\omega_3}{\omega_1}+\frac{\omega_3}{\omega_2}$$

1.10.3. FREQUENCY COMPENSATION:

In applications where one desires large BW and low closed loop gain, suitable compensation techniques are used. Two types are

(i) External compensation
(ii) Internal compensation

(i) External Compensation:

→ Some op-amp are made to be used with externally connected compensating components specially if they are to be used for relatively low closed loop gain.

→ Compensating n/w alters open loop gain so that roll-off is -20dB/decade over a wide range of frequency.

→ Two methods: (a) Dominant pole
(b) Pole-zero (lag)

(a) Dominant pole Compensation:

- 'A' is uncompensated transfer fn. of op-amp in open loop
- Introduce dominant pole by adding RC n/w in series with op amp (or) capacitor 'C' to ground, which have high resistance

Compensated transfer function 'A' becomes,

$$A' = \frac{V_o}{V_i}$$

$$= A \cdot \frac{-j/\omega C}{R - j/\omega C}$$

$$= \frac{A}{1 + jf/f_d}$$

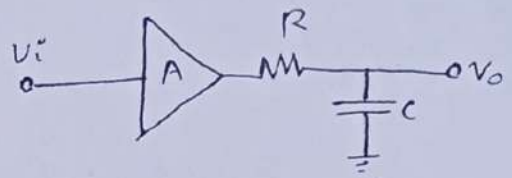


fig Dominant pole compensation

where, $f_d = \frac{1}{2\pi RC}$

$$\therefore A' = \frac{A_{OL}}{\left(1 + j\frac{f}{f_d}\right)\left(1 + j\frac{f}{f_1}\right)\left(1 + j\frac{f}{f_2}\right)\left(1 + j\frac{f}{f_3}\right)} \quad ; f_d < f_1 < f_2 < f_3$$

- Capacitor 'C' is chosen so that modified loop gain drops to 0 dB, with slope of -20dB/decade at frequency where the pole of uncompensated transfer function A contribute negligible phase shift
- $f_d = \frac{\omega_d}{2\pi}$ chosen to make A' pass through 0dB at pole f_1 of uncompensated A

Value of capacitor calculated

$$f = \frac{1}{2\pi RC}$$

Disadvantage:

Reduces open loop bandwidth drastically

Advantage:

noise immunity of system is improved. Since noise from components outside band width are eliminated

Pole Zero compensation:

- Uncompensated transfer fn A is altered by adding both pole & zero
- Zero should be at high frequency than pole
- Transfer fn of compensating nlw is

$$\frac{V_o}{V_2} = \frac{Z_2}{Z_1 + Z_2} = \frac{R_2}{R_1 + R_2} = \frac{1 + j\, f/f_1}{1 + j\, f/f_0}$$

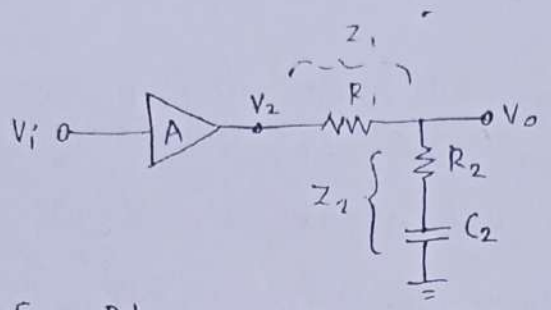
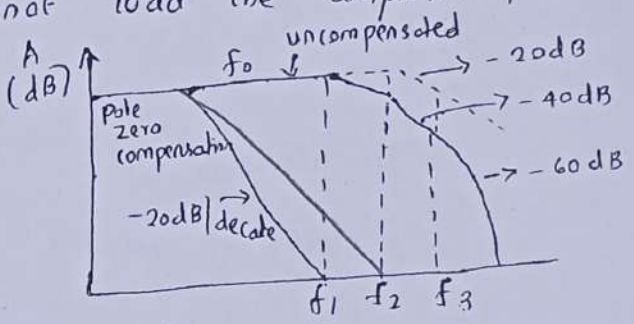


fig. Pole zero compensation

- Compensating n/w is designed to produce zero at 1st corner freq f_1 of uncompensated transfer fn A
- This zero will cancel effect of pole at f_1 Pole at $f_0 = \frac{\omega_0}{2\pi}$ which is selected to A' and is passed through 0dB at f_2 of uncompensated T.F A'.
- Assume compensating n/w doesnot load the amplifier, i.e $R_2 >> R_1$ Overall Transfer fn become



$$A' = \frac{V_o}{V_i} = \frac{V_o}{V_2} \cdot \frac{V_2}{V_i}$$

$$= A \cdot \frac{R_2}{R_1+R_2} \cdot \frac{1+jf/f_1}{1+jf/f_0}$$

$$= \frac{A_{OL}}{\left(1+j\frac{f}{f_1}\right)\left(1+j\frac{f}{f_2}\right)\left(1+j\frac{f}{f_3}\right)} \cdot \frac{R_2}{R_1+R_2} \cdot \frac{1+jf/f_1}{1+jf/f_0}$$

$$= \frac{A_{OL}}{\left(1+j\frac{f}{f_2}\right)\left(1+j\frac{f}{f_3}\right)(1+jf/f_0)} \quad ; 0 < f_0 < f_1 < f_2 < f_3$$

$R_2 >> R_1$ so that $\frac{R_2}{R_1+R_2} \simeq 1$

Now select R_2 & C_2 so that zero of compensating n/w is equal to pole at the freq f_1 (lowest)

(ii) Internally Compensated Op-Amp

- Relatively broad bandwidth of uncompensated op amp is not needed
- Internally compensated op-amps can be used to amplify slow changing signal ∴ doesnot require good high freq response

- Stable regardless of value of closed loop gain
- IC 741 has C_1 of 30 pf internally shunt off signal current and reduce available o/p signal at higher frequencies
- C_1 ⇒ internal compensating ckt, cause open loop gain to roll off at -20dB/ decade & stable ckt
- IC 741 → 1MHz gain bandwidth product

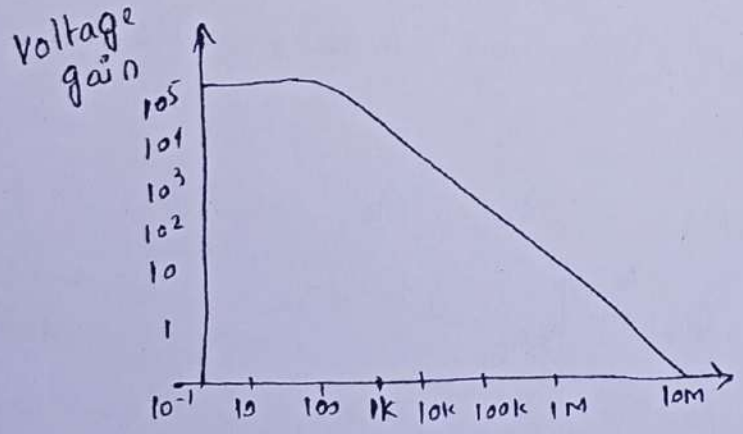


fig. frequency response of μA741 op-amp

SLEW RATE

* The rise time of an amplifier is defined as the time the output takes to change from 10 to 90% of final value for a step i/p 0.35/BW (BW = bandwidth of amplifier).
* Ideal response time should be zero seconds as BW is infinite for ideal op-amp is, output voltage respond to any change in input.
* Rise time is usually specified for small signals, when peak output voltage is less than 1Volt, For large signal output ($V_m > 1V$) opamp's speed is limited by slew rate.
* Opamp's slew rate is related to frequency response.
* opamps with wide bandwidth will have higher (better) slew rates.
* Slew rate is defined as maximum rate of change of output voltage caused by a step input voltage and is usually specified in V/μs.
* An ideal slew rate is infinite which means that op-amp's output voltage change instantaneously in response to input step voltage
* Practical opamp slew rate is 0.1V/μs to above 1000 V/μs.
* Slew rate improves with higher closed loop gain and dc supply voltage, also function of temperature and decreases with an increase in temperature.

Causes of Slew Rate :-

* Capacitor within/outside op amp prevents oscillation, ext. This capacitor prevents output voltage immediately to fast changing input. The rate at which voltage across capacitor increases is

$$\frac{dv_c}{dt} = \frac{I}{C}$$

I = maximum current furnished by op amp to capacitor C

* For obtaining faster slew rate, op-amp should have higher current small compensating capacitor

For 741, $I = 15\mu A$.

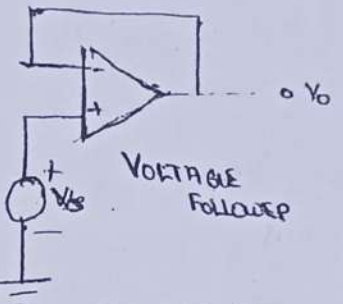
$$SR = \left.\frac{dV_c}{dt}\right|_{max} = \frac{I_{max}}{C} = \frac{15\mu A}{30pF} = 0.5\ V/\mu s.$$

* Slew rate limits the response speed of all large signal waveshapes

* For sine wave input, effect of slew rate

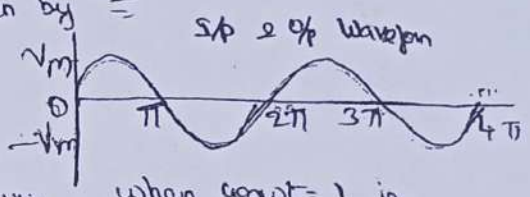
if, $V_s = V_m \sin \omega t$.

Then o/p, $V_o = V_m \sin \omega t$.



* The rate of change of output is given by

$$\frac{dV_o}{dt} = V_m \omega \cos \omega t.$$



* Maximum rate of change of output occurs when $\cos \omega t = 1$ i.e.

$$SR = \left.\frac{dV_o}{dt}\right|_{max} = \omega V_m.$$

Therefore, Slew rate $= 2\pi f V_m$ V/s

$$= \frac{2\pi f V_m}{10^6} \ V/\mu s.$$

where f = input frequency (Hz)

V_m = peak output amplitude

* If frequency / amplitude of input signal is increased to exceed slew rate of op amp, output will be distorted.

* Thus, maximum input frequency f_{max} at which we obtain undistorted output voltage of peak value V_m is given by

$$f_{max}\ (Hz) = \frac{\text{Slew Rate}}{6.28 \times V_m} \times 10^6$$

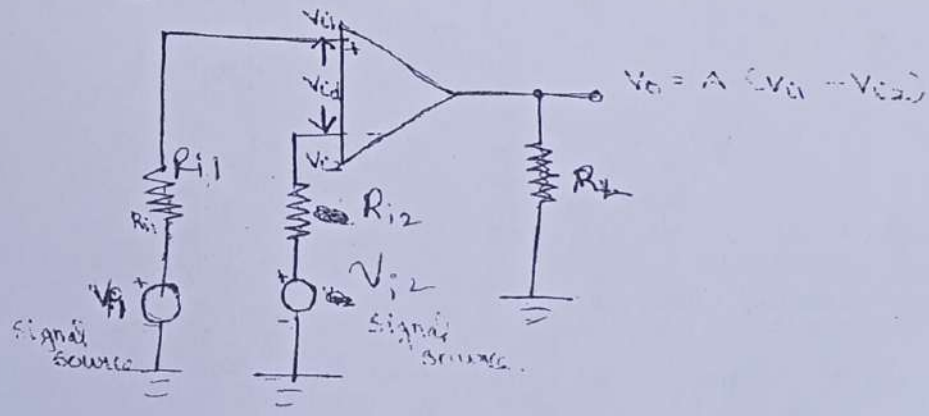
f_{max} = full power response. It is maximum frequency of a large amplitude sine wave with which op amp can have without distortion.

OPEN LOOP OP AMP CONFIGURATION:-

* Open loop indicates no feedback from output to input.
* When connected in open-loop, op amp functions as a very high gain amplifier.
* 3 open loop configuration of op amp: [based on no of i/p's used]
  - Differential amplifier
  - Inverting amplifier
  - Non-inverting amplifier.
* Op-amp amplifies both ac and dc input signals. so input can be ac or dc voltages

OPEN LOOP DIFFERENTIAL AMPLIFIER:-

* In this configuration, inputs are applied to both inverting and non-inverting input terminals of the op-amp and it amplifies the difference between two input voltage.



OPEN LOOP DIFFERENTIAL AMPLIFIER

* The input voltages are represented by V_{i1} and V_{i2}. The source resistance R_{i1} and R_{i2} are negligibly small in comparison with the very high input resistance offered by op amp thus voltage drop across these source resistances is assumed to be zero.
* The output voltage V_o is given by

$$V_o = A(V_{i1} - V_{i2})$$

Voltage gain (A) = Output voltage

A times difference b/n 2 inputs voltage.

* Large signal voltage gain A is called Open loop gain A.

⇒ INVERTING AMPLIFIER :-

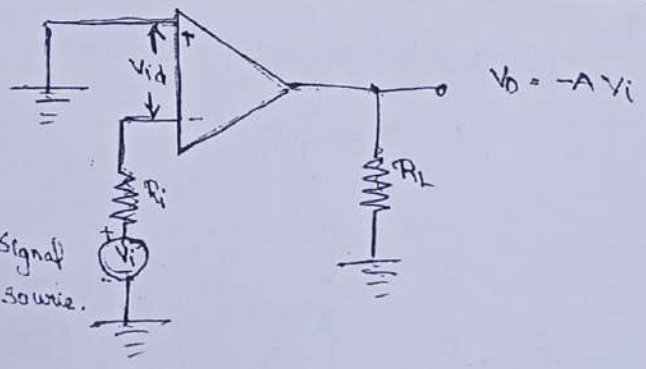
* In this configuration, input signal is applied to the inverting input terminal of op-amp. and non-inverting input terminal is connected to the ground.

* The output voltage is 180° out-of-phase with respect to the input and output voltage V_0 is

$$V_0 = -AV_i$$

* Thus, in an inverting amplifier, the input signal is amplified by open loop gain A and phase shifted by 180.

OPEN LOOP INVERTING AMPLIFIER.



⇒ NON-INVERTING AMPLIFIER :-

* The input signal is applied to the non-inverting input terminal of the op-amp and inverting input terminal is connected to the ground.

* Input signal is amplified by open-loop gain A. and output is in phase with the input signal

$$V_0 = AV_i$$

* Voltage level slightly greater than zero, output is driven into saturation.

either in negative or positive saturation or switches between both. This prevents the use of open loop configuration of op-amps in linear application

⇒ LIMITATIONS OF OPEN LOOP OP-AMP CONFIGURATION :-

* clipping of output waveform occur due to output voltage exceeds the saturation level of op-amp.
* Due to very high open-loop gain of op-amp. This makes to possible to amplify very low frequency signal (mV or even less) & amplification done accurately without any distortion.
* open-loop gain of op-amp is not constant & varies with changing temperature & variation in power supply.
* Bandwidth of open loop op-amp is negligibly small. These makes open loop
* conf. unsuitable for AC applications.
* IC741 - B.W = 5Hz
* open loop configuration not used in linear applications. In non-linear applications such as comparator, square wave generators & astable multivibrators.

CLOSED LOOP OP-AMP CONFIGURATIONS :-

* Op-amp utilize in linear application by providing a feedback from output to input.
* If signal feedback is out-of phase by 180° w.r.t to input then feedback is referred to as "Negative feedback" or "Degenerative feedback".
* If signal feedback is in-phase with that of input, then feedback is referred to as "Positive feedback" or "Regenerative feedback".
* Op-amp that uses feedback is called a CLOSED LOOP AMPLIFIER

↳ Inverting amplifier (voltage - shunt feedback)

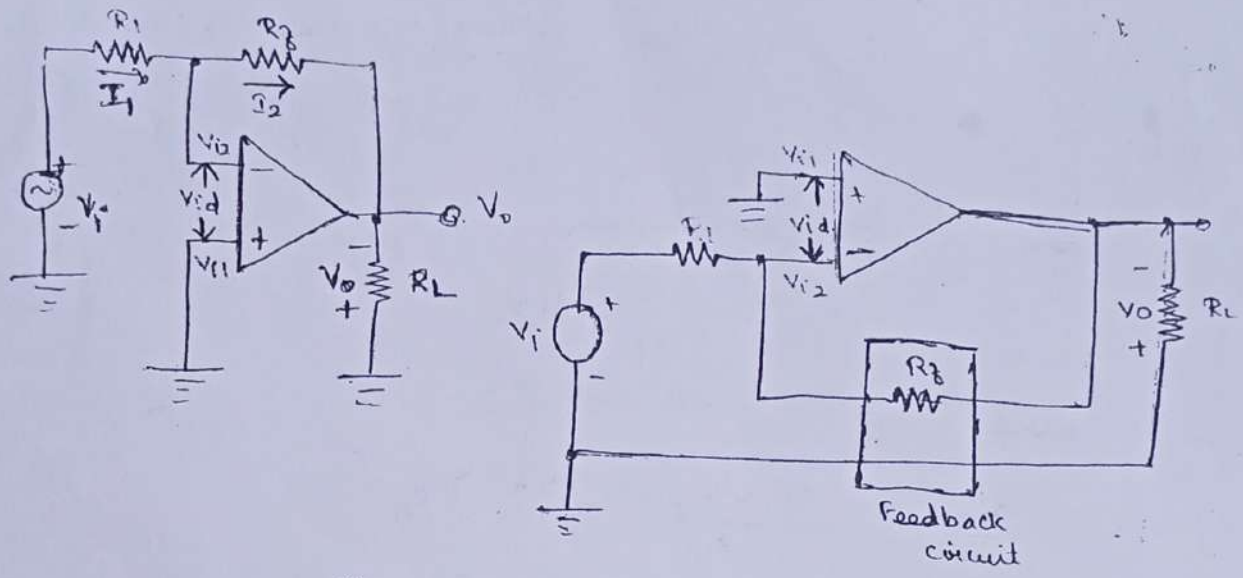
↳ Non inverting amplifier (voltage - Series feedback)

↳ INVERTING AMPLIFIER :-

* Input signal drives the inverting input of ~~op amp open loop~~ gain op amp through resistor R_1
* Op amp has an open loop gain of A, o/p signal is much larger than the error voltage.
* Because of Phase inversion, output signal is out of phase 180° with input signal.
* Feedback signal opposes the input signal and the feedback is negative / degenerative.

* VIRTUAL GROUND :

* Virtual ground is a ground which acts like a ground. May not have physical connection to ground. This property of an ideal Op amp indicates that inverting & non-inverting terminals of op amp are same potential.
* Non-inverting input is grounded for inverting amplifier, so inverting input of op-amp is also at ground potential.
* Virtual ground is at fixed ground potential (or).
* Input current is so small so approx to zero.
* I/p voltage applied at inverting i/p, V_{id} = differential voltage is negligibly small, $I_D = 0$ so, inverting input act as virtual ground.
* Virtual Ground : whose voltage with respect to ground is zero, but no current can flow on it



CLOSED LOOP INVERTING AMPLIFIER.

* $Z_i = R_i$ (∵ inv i/p = virtual ground)

$$\therefore I_1 = \frac{V_i}{R_1}$$

* This current must flow through R_f, bcoz, virtual ground accepts ngligible current

$$V_o = -I_2 R_f = -\frac{R_f}{R_1} V_i$$

closed loop voltage gain A_V,

$$A_V = \frac{V_o}{V_i} = -\frac{R_f}{R_1}$$

NON-INVERTING AMPLIFIER

* Input signal drives non-inverting i/p of op-amp. Op-amp provides an internal gain A
* External resistors R_1 & R_f form the feedback voltage divider ckt with an attenuation factor of B
* Feedback voltage is at inverting i/p, it opposes i/p voltage at the non-inverting i/p terminal, so feedback is negative/degenerative.

differential voltage Vid at the input of the op-amp is zero, i.e. at node a, is at same voltage as that of non-inv i/p terminal

* R_1 & R_2 form a potential divider,

$$\therefore V_i = \frac{R_1}{R_1+R_2} \times V_o$$

do no current flow into op-amp

$$\frac{V_o}{V_i} = \frac{R_1+R_2}{R_1} = 1 + R_2/R_1$$

$\therefore$ Voltage gain for non inv amplifier is

$$A_V = \frac{V_o}{V_i} = 1 + \frac{R_2}{R_1}$$

* Feedback factor of the feedback voltage divider network

$$\beta = \frac{R_1}{R_1+R_2}$$

$\therefore$ closed loop gain is

$$A_V = 1/\beta = \frac{R_1+R_2}{R_1}$$

$$A_V = 1 + R_2/R_1$$

A_V always $\gg 1$. : depends on ratio of feedback resistance

* closed loop gain doesn't drift with temperature change or op amp replacement.

* Input resistance of the op amp is extremely large.

EC8453 - LIC

Unit II - Applications of Operational Amplifiers

Syllabus:

Sign changer - scale changer - phase shift ckt, voltage follower - V to I & I to V converters, adder, subtracter, Instrumentation amplifier, Integrator, Differentiator, Logarithmic amplifier, Antilogarithmic amplifier, comparators, Schmitt trigger, precision rectifier, peak detector, clippers & clampers, low-pass, high-pass and band-pass butterworth filters

Introduction: (WWW - What, Why, Where)

① What does this unit deals about?

as we have discussed about electronics of op-amp (ac/dc characters, limitations, open/closed loop configuration), we take a look at the applications of an op-amp.

② Why we study this?

→ op-amp has countless applications which form basic building block of analog s/m (both linear & non-linear)

→ Linear applications (Topics like differentiator)

→ non-linear applications (: Hill filters)

③ Where this unit applied in practice?

They are very useful in industrial instrumentation, communication & general signal processing.

2.1 Sign changer (Phase Inverter)

The basic inverting amp configuration using an op-amp with i/p impedance Z_1 and feedback impedance Z_f is shown.

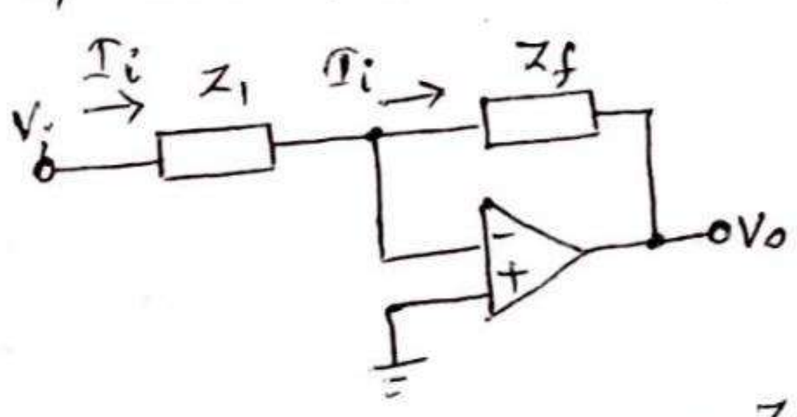


fig. inverting op-amp with shunt f/b

- closed loop voltage gain : $-\frac{Z_f}{Z_1}$
- Impedance Z_1 & Z_f are equal in magnitude & phase, then closed loop voltage gain is -1.

→ which cause 180° phase shift at o/p → is called as "phase inverter"

2.2 Scale changer

- Referring to the same above fig., if ratio $Zf/Z_1 = K$, a real constant, then closed loop gain is $-K$
- I/p voltage is multiplied by $-K$
- Scaled o/p is available at o/p
- In such applications, Zf & Z_1 are selected as precision resistors for obtaining precise & scaled value of i/p voltage.

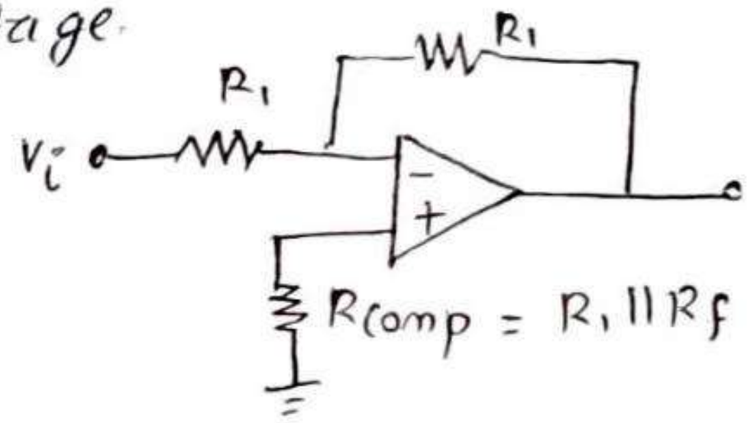


fig. Scale changer

2.3 Phase shift circuits:

- produce phase shift depends on frequency & maintain constant gain
- Also called as "Constant-delay filters" or "all pass filters"
- Diff b/w i/p & o/p voltage remain constant when freq is changed over operating freq.

(a) Phase lag ckt

- Constructed by connecting both inverting & non-inverting modes
- Assume i/p voltage V_i drive simple inverting amp
- Inverting gain $= -1$
- non-inverting gain $= 1 + \frac{Rf}{R_1}$

$= 1 + 1$

$= 2 \quad (\because Rf = R_1)$

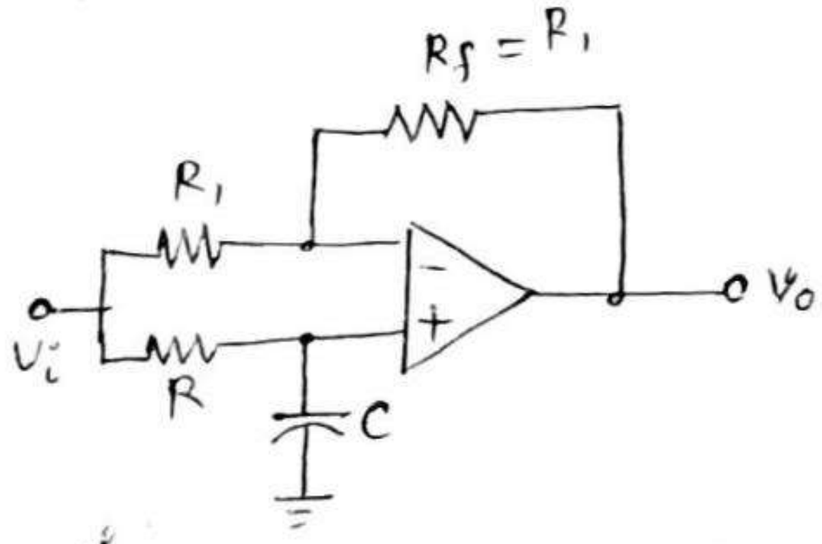


Fig. phase lag ckt

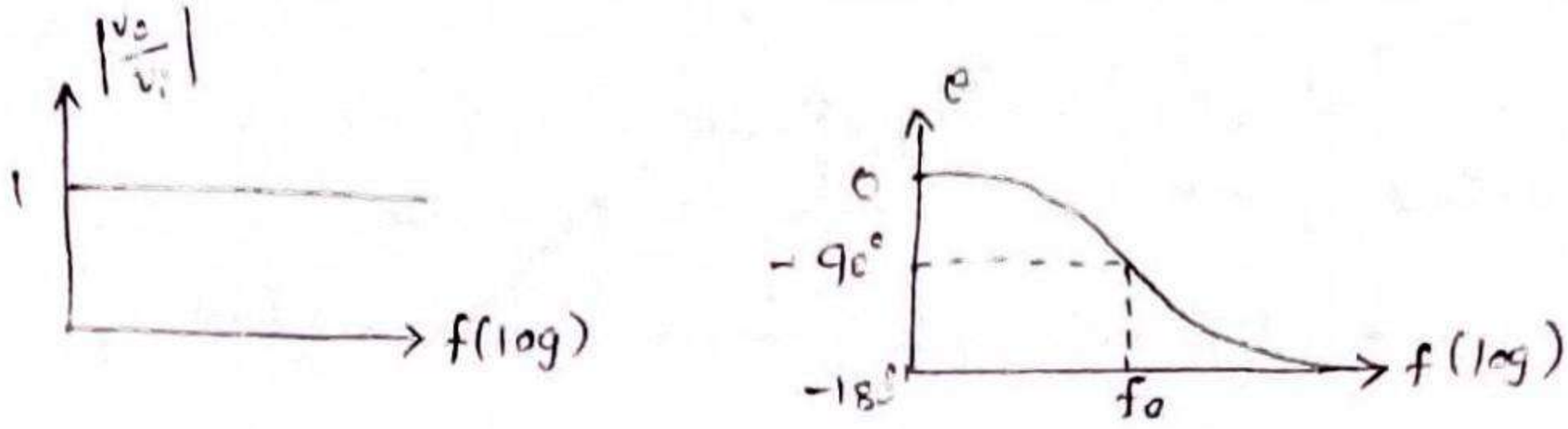


fig Bode plot for phase lag ckt

From ckt,

$$V_o(j\omega) = -V_i(j\omega) + 2\,\frac{1}{1+j\omega RC}\,V_i(j\omega) \qquad \rightarrow (1)$$

$$= V_i(j\omega)\left[-1 + \frac{2}{1+j\omega RC}\right]$$

$$= V_i(j\omega)\left[\frac{-1-j\omega RC+2}{1+j\omega RC}\right]$$

$$\therefore \quad V_o(j\omega) = V_i(j\omega)\left[\frac{1-j\omega RC}{1+j\omega RC}\right]$$

The relationship b/w o/p & i/p can be expressed by

$$\frac{V_o(j\omega)}{V_i(j\omega)} = \frac{1-j\omega RC}{1+j\omega RC} \qquad \rightarrow (2)$$

The phase angle is given by

$$\theta = -\tan^{-1}(\omega RC) - \tan^{-1}(\omega RC) = -2\tan^{-1}(\omega RC) \qquad \rightarrow (3)$$

When $\omega = 0$, phase angle approaches zero

$\omega = \infty$, " " $-180°$

$$(3) \Rightarrow \boxed{\theta = -2\tan^{-1}(f/f_c)} \qquad \rightarrow (4)$$

where, $f_c = \frac{1}{2\pi RC}$ $\qquad \rightarrow (5)$

When $f = f_c$ in eqn (4), phase angle $\theta = -90°$

(b) Phase-lead ckt

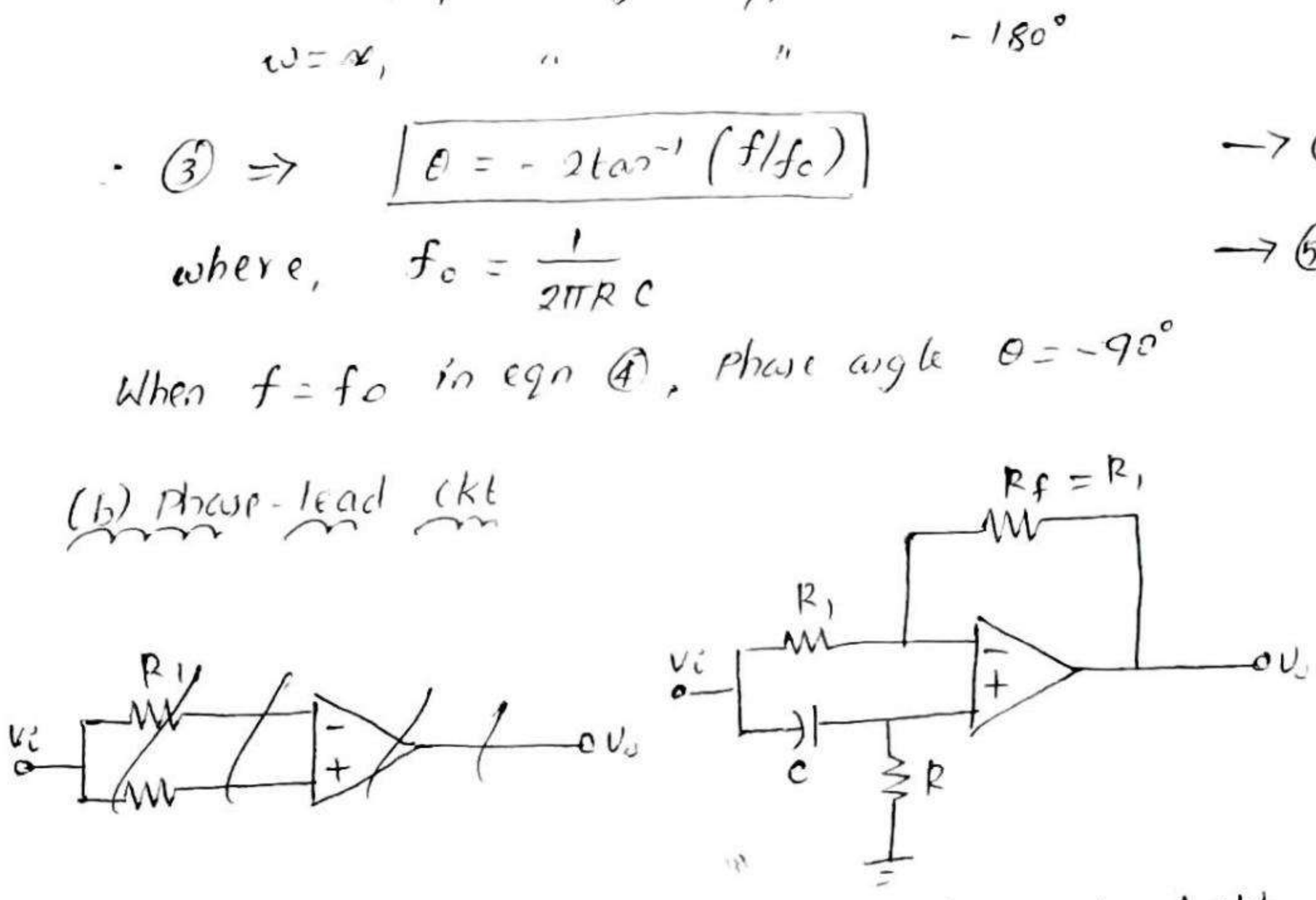
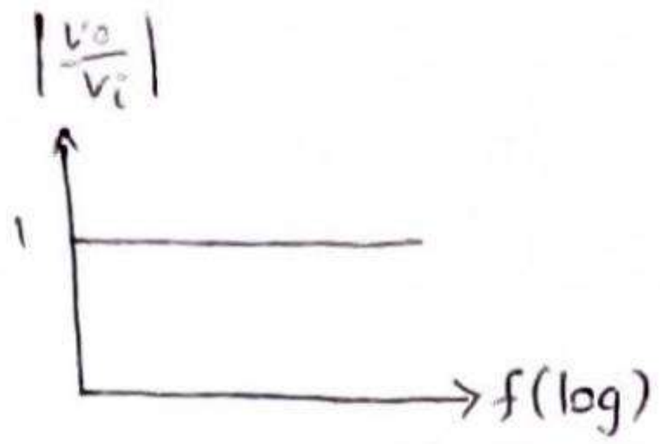


fig. phase-lead ckt



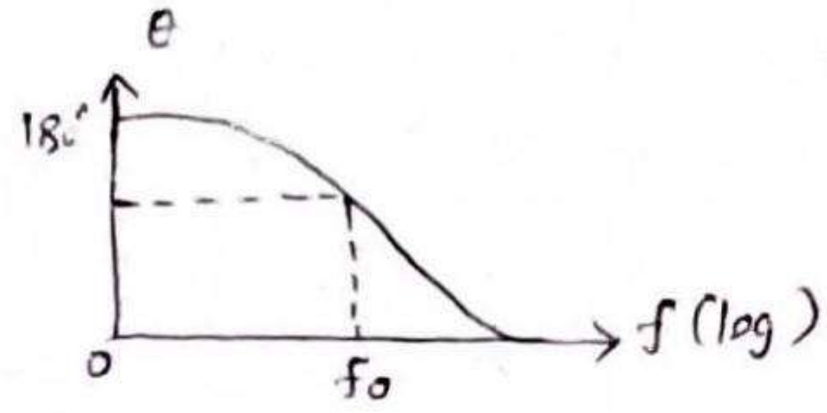


fig (b) Bode plot for phase-lead ckt

- Ckt ⇒ RC ckt form high pass n/w
- o/p voltage is derived by

$$V_o(j\omega) = -V_i(j\omega) + 2\left(\frac{j\omega RC}{1+j\omega RC}\right) V_i(j\omega)$$

$$\therefore \quad \frac{V_o(j\omega)}{V_i(j\omega)} = \frac{-1+j\omega RC}{1+j\omega RC} \longrightarrow (6)$$

Eqn (6) → ratio of magnitude is constant & phase is obtained as in eqn (3). It is to be noted that Nr has a -ve real part & overall phase is

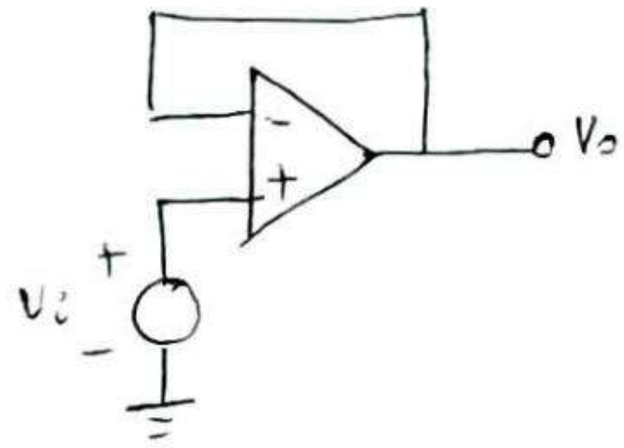
$$\theta = 180^\circ - \tan^{-1}(\omega RC) - \tan^{-1}(\omega RC)$$

$$= 180^\circ - 2\tan^{-1}(\omega RC) \longrightarrow (7)$$

- Frequency → 0, phase angle → 180°
- Freq ↑, leading phase ↓ & finally → 0 at high freq
- Eqn (7) → $\boxed{\theta = 180^\circ - 2\tan^{-1}(f/f_o)}$ → (8)

where, $f_o = \frac{1}{2\pi RC}$

4 Voltage follower :-



- If $R_1 = \infty$, $R_f = 0$ in non-inverting amplifier, then amplifier acts as a unity-gain amplifier or voltage follower

  i.e $A_v = 1 + \frac{R_f}{R_1}$ (or) $\frac{R_f}{R_1} = A_v - 1$

  Since, $\frac{R_f}{R_1} = 0$, we have $A_v = 1$

- o/p voltage = i/p voltage, both in magnitude & phase ($V_o = V_i$)
- Since o/p follows i/p voltage, it is called as voltage follower
- Also referred as Source follower, buffer amplifier, isolation amplifier, unity gain amplifier
- High i/p impedance of MΩ, low o/p impedance
- Used as a buffer b/w a high impedance source & a low impedance matching applications

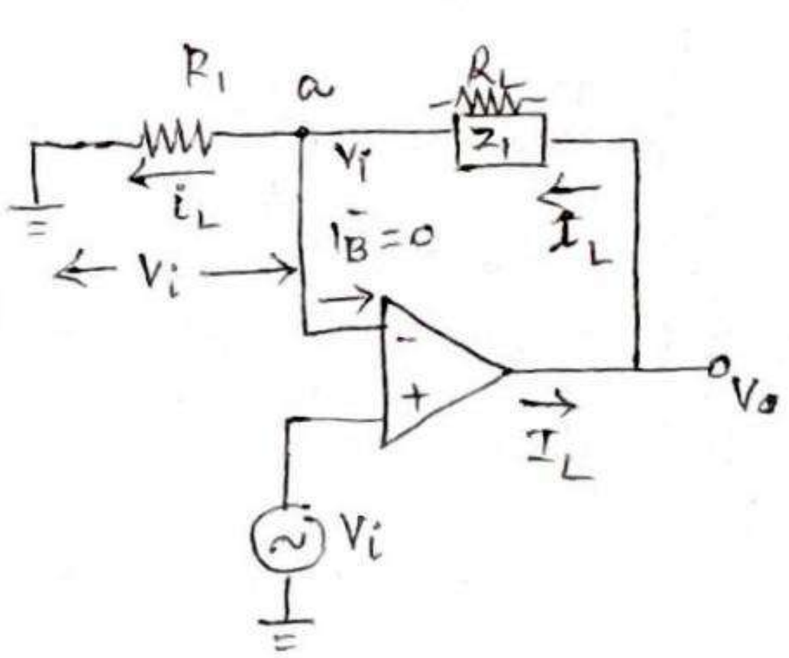
2.5 V-to-I and I-to-V Converters:

(a) Voltage to current converter (Transconductance amplifier)

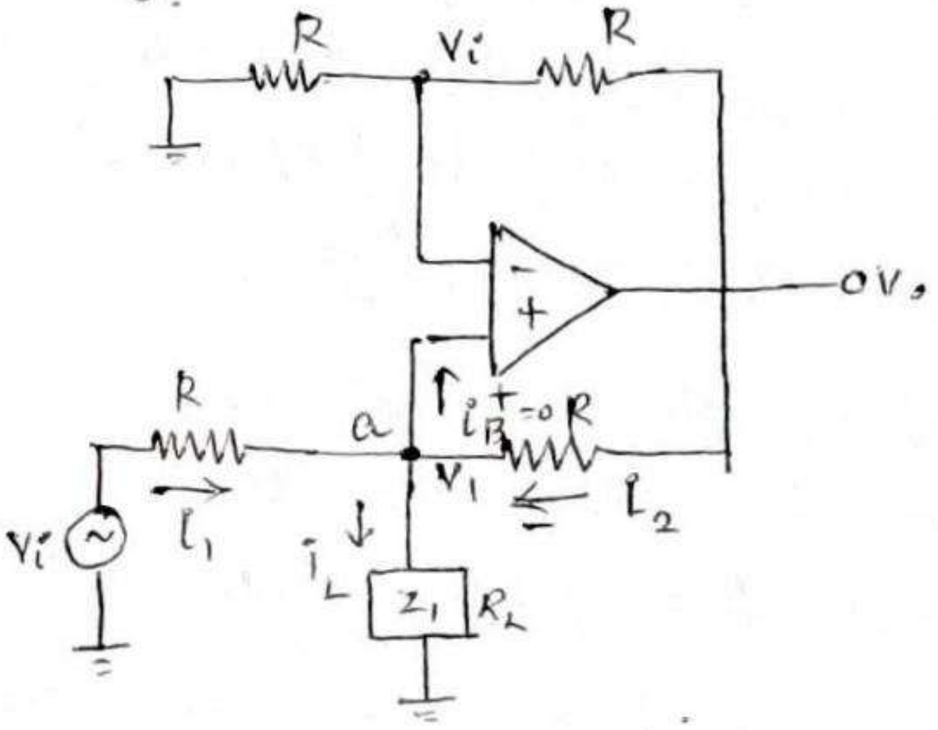
To convert voltage signal to a proportional o/p current, 2 types of circuits can be considered

(i) V-I Converter with floating load

(ii) V-I Converter with grounded "



fig(a) floating load



fig(b) grounded load

→ Fig(a) show voltage to current converter in which load Z_L is floating

Voltage at node 'a' is V_i

$$V_i - i_L R_1 \quad (\text{as } I_B = 0)$$

(or) $$\boxed{i_L = \frac{V_i}{R_1}}$$

- I/p voltage V_i is converted as o/p current of V_i/R_1

→ Fig(b) show V-I converter with grounded load. Let V_1 be the voltage at node 'a'

Apply KVL $\Rightarrow$ $i_1 + i_2 = i_L$

$$\frac{V_i - V_1}{R} + \frac{V_o - V_1}{R} = i_L$$

$$V_i - 2V_1 + V_o = i_L R$$

$$\therefore \quad \boxed{V_1 = \frac{V_i + V_o - i_L R}{2}}$$

∵ op amp is in non-inverting mode, gain is $1 + \frac{R}{R} = 2$

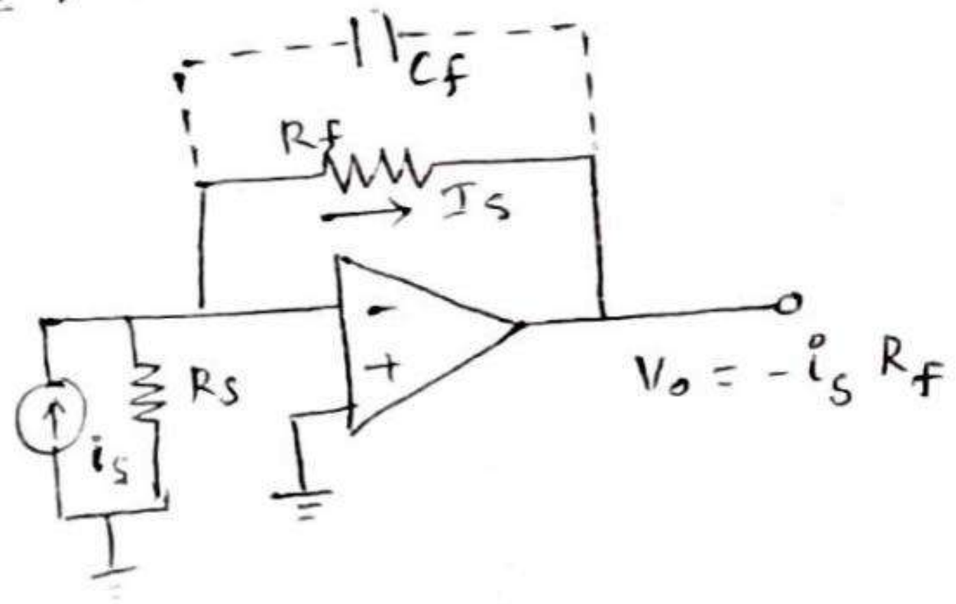
The o/p voltage, $V_o = 2V_1 = V_i + V_o - i_L R$

that is, $V_i = i_L R$

$$\Rightarrow \boxed{i_L = V_i/R}$$

(b) Current to voltage converter (Transresistance amplifier)

- Photo cell, photodiode, photovoltaic cell gives an o/p current that is proportional to incident radiant energy / light



- Current through these devices is converted to voltage using I to V converter, thereby light is measured

- Op-amp is used as I to V converter
- '−' i/p terminal → virtual ground, no current flow through R_s & is current flow through feedback resistor R_f

- $V_o = -i_s R_f$
- lowest current that this ckt can measure will depend upon bias current I_B of op amp i.e μA741 (I_B - 80nA) can be used to detect lower current
- Sometimes, R_f is shunted with capacitor C_f to reduce high frequency noise & possibility of oscillation

2.6 Adder / Summing Amplifier

- Op-amp maybe used to design a ckt whose o/p is sum of several i/p sgnls which is known as "Summing amplifier" (or) "Summer"
- Inverting & non-inverting Summer are discussed as follows:

(a) Inverting Summing amplifier

- Summing amplifier with 3 i/p voltage V_1, V_2, V_3, 3 i/p resistors R_1, R_2 & R_3 and a feedback resistor R_f is shown below

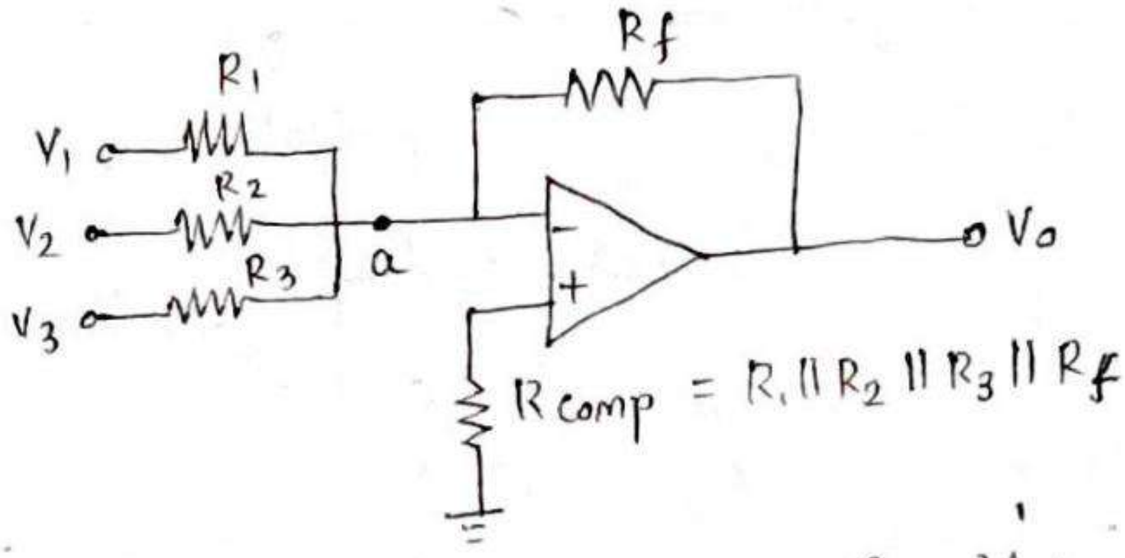


fig Inverting Summing amplifier

- On analysing, assume op-amp is ideal. i.e $A_{OL} = \infty$, $R_i = \infty$
- I/p bias current assumed to be zero, no voltage drop across Rcomp non-inverting terminal is grounded
- Voltage at node "a" is zero as non-inverting terminal is grounded

Nodal eqn. by KCL at "a"

$$\frac{V_1}{R_1} + \frac{V_2}{R_2} + \frac{V_3}{R_3} + \frac{V_o}{R_f} = 0$$

$$V_o = -\left[\frac{V_1 R_f}{R_1} + \frac{V_2 R_f}{R_2} + \frac{V_3 R_f}{R_3}\right]$$

- Thus o/p is inverted & weighted sum of i/ps. This special case, when $R_1 = R_2 = R_3 = R_f$, we have

$$\boxed{V_o = -(V_1 + V_2 + V_3)}$$

in which o/p is inverted sum of i/p sgnls. We may also set $R_1 = R_2 = R_3 = 3R_f$, in which

$$\boxed{V_o = -\left(\frac{V_1 + V_2 + V_3}{3}\right)}$$

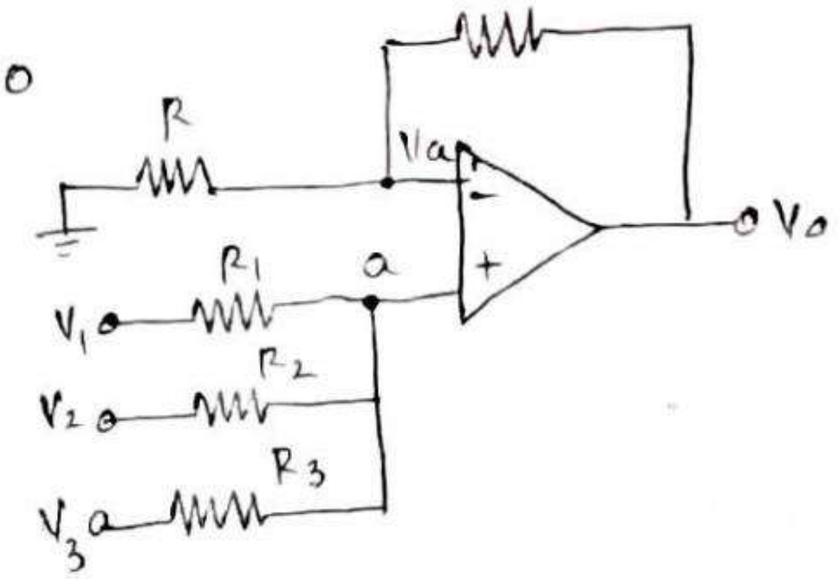
- Thus o/p is average of i/p sgnl (inverted)

Effective resistance, $R_i = R_1 \| R_2 \| R_3$

$\therefore R_{comp} = R_i \| R_f = R_1 \| R_2 \| R_3 \| R_f$

(b) Non inverting summing amplifier:

- Summer that gives a non-inverted sum is non-inverting summing amplifier.
- Let voltage at '−' i/p terminal be Va
  Voltage at '+' i/p terminal also Va
- The nodal eqn at node 'a' is given by



$$\frac{V_1 - V_a}{R_1} + \frac{V_2 - V_a}{R_2} + \frac{V_3 - V_a}{R_3} = 0$$

$$\Rightarrow \boxed{V_a = \frac{\frac{V_1}{R_1} + \frac{V_2}{R_2} + \frac{V_3}{R_3}}{\frac{1}{R_1} + \frac{1}{R_2} + \frac{1}{R_3}}}$$

- The op-amp & 2 resistors R_f & R constitute a non-inverting amplifier with $V_o = \left(1 + \frac{R_f}{R}\right) V_a$

$\therefore$ o/p voltage is $\boxed{V_o = \left(1 + \frac{R_f}{R}\right) \frac{\left(\frac{V_1}{R_1} + \frac{V_2}{R_2} + \frac{V_3}{R_3}\right)}{\left(\frac{1}{R_1} + \frac{1}{R_2} + \frac{1}{R_3}\right)}}$

which is non-inverted weighted sum of i/p

Let $R_1 = R_2 = R_3 = R = R_f/2$

then, $\boxed{V_o = V_1 + V_2 + V_3}$

A basic diff amplifier used as a Subtractor is shown.

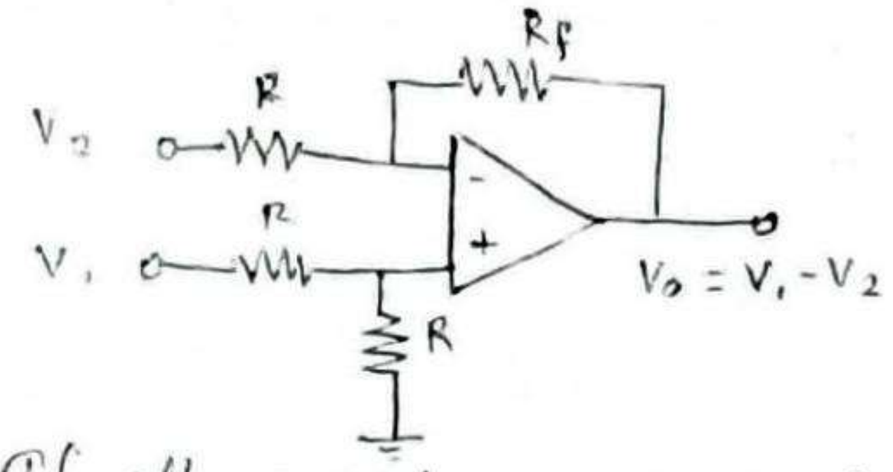


fig Subtractor

- If all resistors are equal, o/p voltage derived by using Superposition principle
- o/p V_{o1} due to V_1, make $V_2 = 0$. ckt becomes non-inverting amplifier having i/p voltage $V_1/2$ at non-inverting i/p terminal & o/p becomes

$$V_{o1} = \frac{V_1}{2}\left(1 + \frac{R}{R}\right) = V_1$$

- Wi'y o/p V_{o2} due to V_2 is

$$V_{o2} = -V_2$$

∴ o/p voltage due to both i/p can be written as

$$\boxed{V_o = V_{o1} + V_{o2} = V_1 \; V_2}$$

Adder-Subtractor

- To perform addition & Subtraction with single op-amp using the ckt shown.

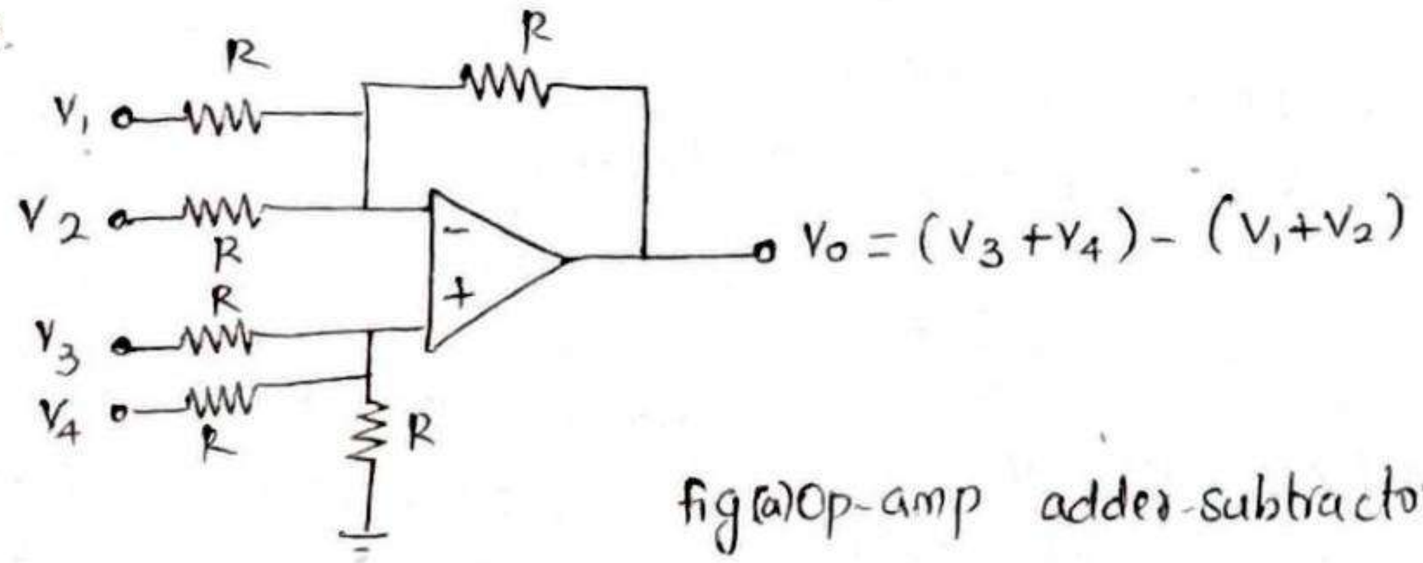


fig (a) Op-amp adder-subtractor

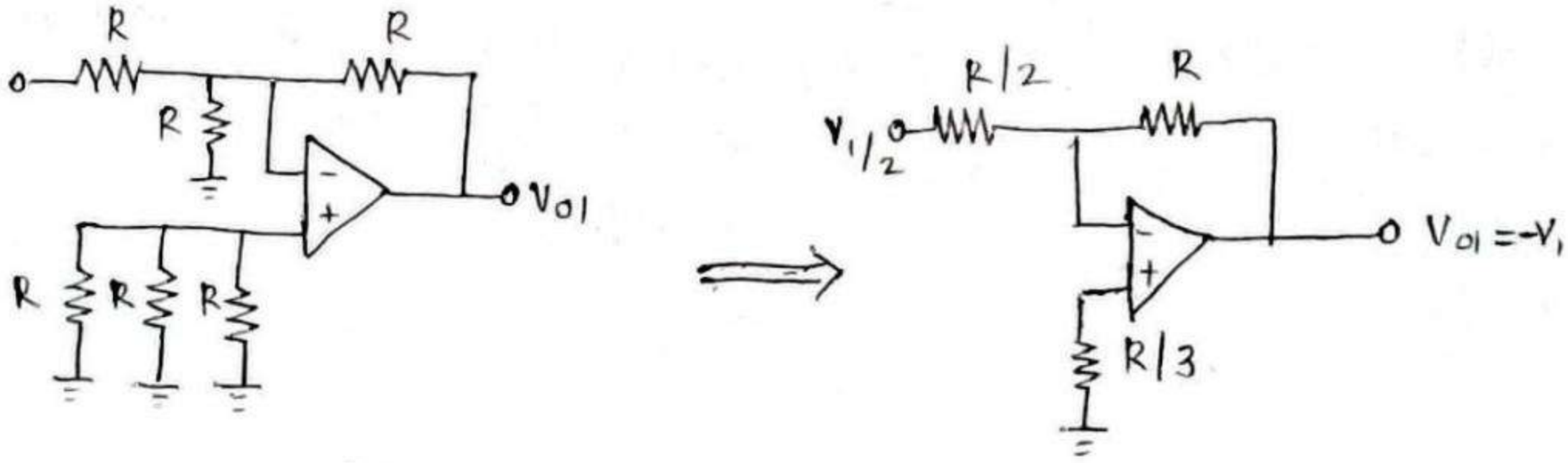


fig (b) Simplifier ckt for $V_2 = V_3 = V_4 = V_o$

- The o/p voltage can be obtained by "Superposition theorem". To find o/p voltage V_{o1} due to V_1, make all other i/p voltage V_2, V_3 & $V_4 = 0$

Fig(b) is the simplified ckt of an inverting amplifier & o/p voltage is, $\frac{V_{o1}}{(V_1/2)} = -\frac{R}{R/2}$ $\left(\because \frac{V_o}{V_i} = -R_f/R\right)$

$$\Rightarrow V_{o1} = -\frac{R}{\frac{R}{2}} \frac{V_1}{2} = -V_1$$

- III'ly by Thevenin's theorem,

$$\boxed{V_{o2} = -V_2}$$

- V_{o3} due to V_3, make other $V_1, V_2, V_4 = 0$ The voltage V_a at non-inverting terminal is,

$$V_a = \frac{R/2}{R + R/2} \cdot V_3 = \frac{V_3}{3}$$

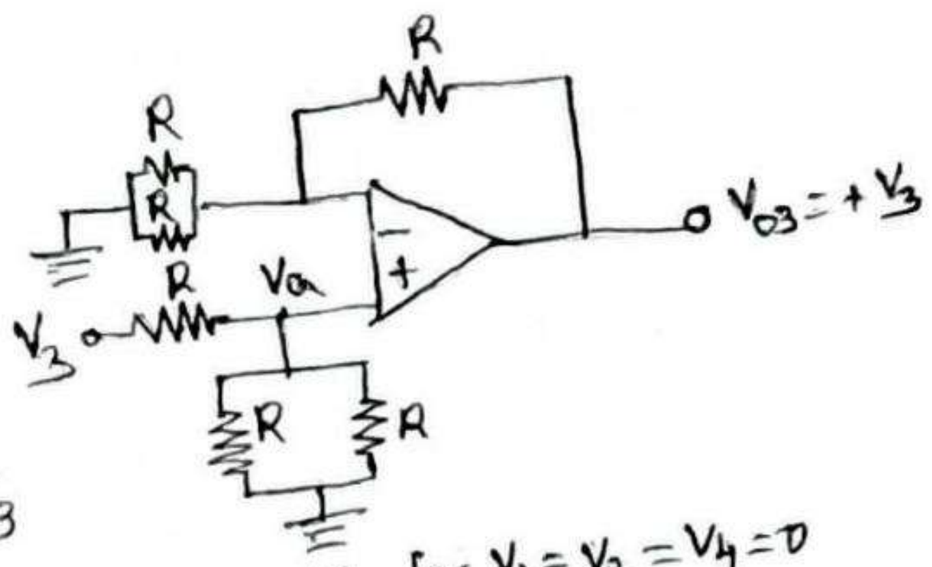


Fig ckt for $V_1 = V_2 = V_4 = 0$

- o/p voltage V_{o3} due to V_3 alone is

$$V_{o3} = \left[1 + \frac{R}{R/2}\right] V_a = 3\left(\frac{V_3}{3}\right) = V_3$$

- III'ly V_{o4} due to V_4 is $\boxed{V_{o4} = V_4}$
- Thus o/p voltage V_o due to all 4 i/p voltages is given by

$$V_o = V_{o1} + V_{o2} + V_{o3} + V_{o4}$$
$$= -V_1 - V_2 + V_3 + V_4$$
$$= (V_3 + V_4) - (V_1 + V_2)$$

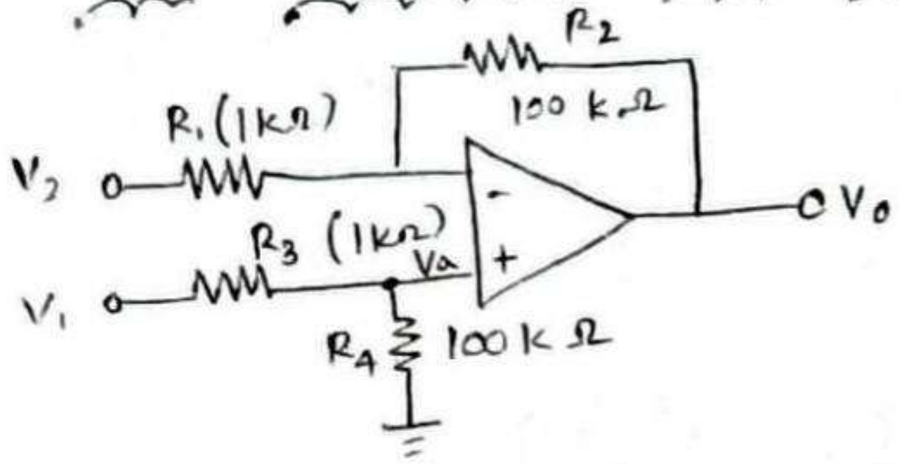
∴ The ckt is an adder - Subtractor

2.7 Instrumentation Amplifier :-

- In industrial / consumer applications, we need to measure & control Physical quantities Some examples are measurement & control of temperature, humidity, light intensity, water flow, etc which are measured with the help of transducers The o/p of transducer has to be amplified so that it can drive the indicator or display s/m This fn is performed by an instrumentation amplifier.

- The important features of Instrumentation amp are
  (i) high gain accuracy
  (ii) high CMRR
  (iii) high gain stability with low temperature co-efficient
  (iv) low dc offset
  (v) low o/p impedance, (vi) high i/p impedance

(1) Consider basic differential amp as shown below



DA using single op. amp

o/p voltage is $V_o = \frac{-R_2}{R_1} V_2 + \frac{1}{1+\frac{R_3}{R_4}} V_1 \left(1+\frac{R_2}{R_1}\right)$

$V_{o2} = \frac{-R_2}{R_1} V_2 \quad \rightarrow (1)$

$V_{o1} = \left(1+\frac{R_2}{R_1}\right) V_a \quad \rightarrow (2)$

where, $V_a = \frac{R_4}{R_3+R_4} V_1 \rightarrow (3)$

(3) in (2) $V_{o1} = \left(1+\frac{R_2}{R_1}\right) V_1 \left(\frac{R_4}{R_3+R_4}\right) \rightarrow (4)$

We know o/p voltage is $\boxed{V_o = V_{o1} + V_{o2}} \rightarrow (5)$

Sub (1) & (4) in (5).

$$V_o = \frac{-R_2}{R_1} V_2 + \left(1+\frac{R_2}{R_1}\right) V_1 \left(\frac{R_4}{R_3+R_4}\right)$$

$$= \frac{-R_2}{R_1} V_2 + \left(1+\frac{R_2}{R_1}\right) V_1 \left(\frac{1}{\frac{R_3+R_4}{R_4}}\right)$$

$$= \frac{-R_2}{R_1} V_2 + \left(1+\frac{R_2}{R_1}\right) V_1 \left(\frac{1}{\frac{R_3}{R_4}+1}\right)$$

$$\therefore V_o = \frac{-R_2}{R_1}\left[V_2 - \left(\frac{R_1}{R_2}+1\right) V_1 \left(\frac{1}{R_3/R_4+1}\right)\right] \rightarrow (6)$$

If $\frac{R_1}{R_2} = \frac{R_3}{R_4}$

$$\Rightarrow V_o = -\frac{R_2}{R_1}\left[V_2 - \left(\frac{R_1}{R_2}+1\right)\left(\frac{1}{\frac{R_1}{R_2}+1}\right) V_1\right]$$

$$V_o = -\frac{R_2}{R_1}(V_2 - V_1) = \frac{R_2}{R_1}(V_1 - V_2) \rightarrow (7)$$

Drawbacks of single RA IA:

(i) $R_1 = R_3$ & $R_2 = R_4$

i/p voltage $\Rightarrow$ $(R_3 + R_4)$ for V_1

R_1 for V_2

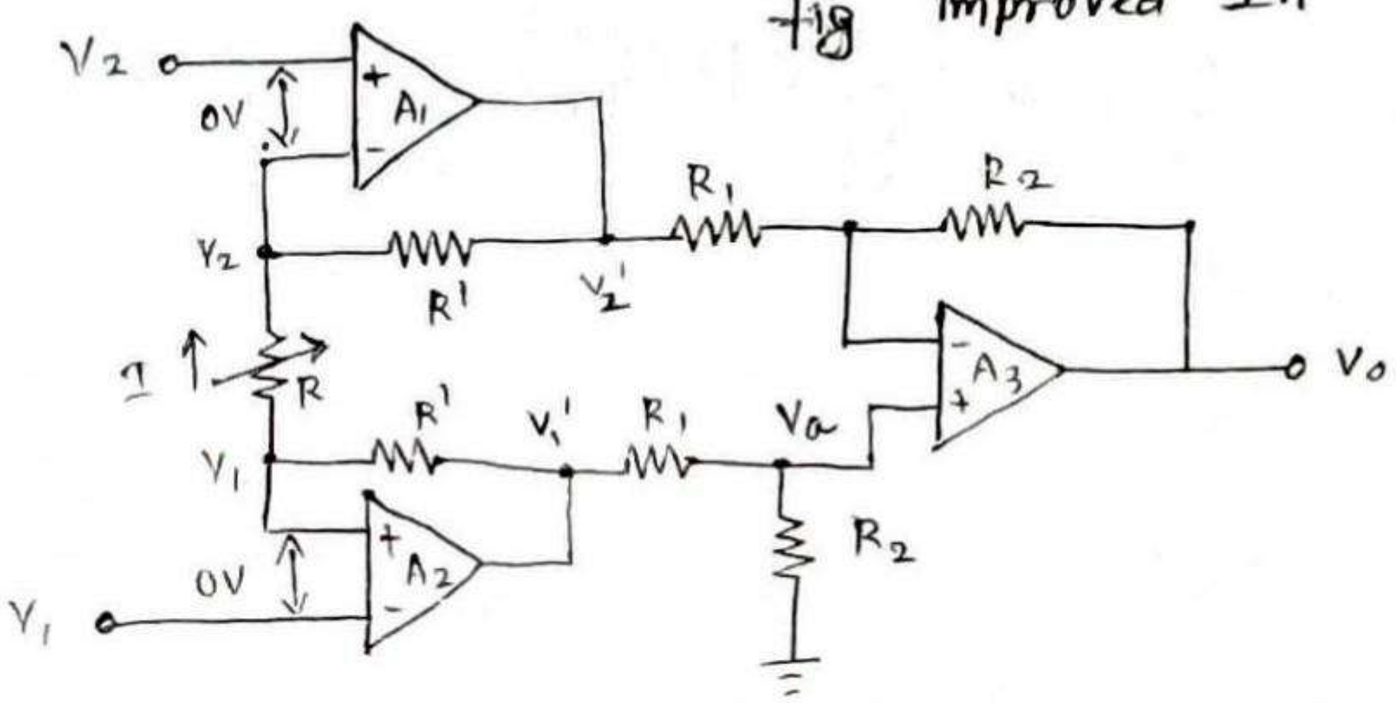
$\therefore (R_3 + R_4) >> R_1$

o/p V_1 is heavily loaded bcz of low impedance

(ii) gain R_2/R_1 is insufficient for high gain applications

(2) Three Op amp or Improved instrumentation amplifier

fig Improved IA



- Op amp A_1, A_2 : $\boxed{V_d = 0}$, for $V_1 = V_2$ i.e under common mode, voltage across 'R' is zero

(a) no current flow through R & R', A_1 acts as voltage follower

$\therefore V_1' = V$ & $V_2' = V_2$

(b) If $V_1 \neq V_2$, current flows through R & R', $(V_2' - V_1') > (V_2 - V_1)$

high CMRR

- Voltage at '+' terminal of A_3 $\boxed{V_a = \frac{R_2}{R_1 + R_2} V_1'}$ (Superposition theorem) $\rightarrow$ (8)

- Here, $V_{02} = -\frac{R_2}{R_1} V_2'$ $\rightarrow$ (9)

$V_{01} = \left(1 + \frac{R_2}{R_1}\right) V_a$ $\rightarrow$ (10)

Sub (8) in (10)

$\Rightarrow V_{01} = \left(1 + \frac{R_2}{R_1}\right)\left(\frac{R_2}{R_1 + R_2}\right) V_1'$ $\rightarrow$ (11)

$\therefore$ o/p voltage $V_o = V_{01} + V_{02}$

$\Rightarrow V_o = \left(1 + \frac{R_2}{R_1}\right)\left(\frac{R_2}{R_1 + R_2}\right) V_1' - \frac{R_2}{R_1} V_2'$

$$V_o = \frac{R_2}{R_1} V_2' + \left(\frac{R_1 + R_2}{R_1}\right)\left(\frac{R_3}{R_3 + R_4}\right) V_1'$$

$$= \frac{R_2}{R_1} V_2' + V_1' \frac{R_2}{R_1}$$

$$\boxed{V_o = \frac{R_2}{R_1}(V_1' - V_2')} \longrightarrow (12)$$

(c) 'I' flows in 'R' $\Rightarrow$ $\boxed{I = (V_1 - V_2)/R}$ $\longrightarrow (13)$

$$V_1' = IR' + V_1 = R'\left(\frac{V_1 - V_2}{R}\right) + V_1$$

$$\boxed{V_1' = \frac{R'}{R}(V_1 - V_2) + V_1} \longrightarrow (14)$$

$$V_2' = -IR' + V_2 = R'\left(\frac{V_1 - V_2}{R}\right) + V_2$$

$$\boxed{V_2' = \frac{-R'}{R}(V_1 - V_2) + V_2} \longrightarrow (15)$$

WKT, $V_o = \frac{R_2}{R_1}(V_1' - V_2')$ from eqn (12)

$$= \frac{R_2}{R_1}\left[\left(\frac{R'}{R}(V_1 - V_2) + V_1\right) - \left(\frac{-R'}{R}(V_1 - V_2) + V_2\right)\right]$$

$$= \frac{R_2}{R_1}\left[\frac{R'}{R}(V_1 - V_2) + V_1 + \frac{R'}{R}(V_1 - V_2) - V_2\right]$$

$$= \frac{R_2}{R_1}\left[2\frac{R'}{R}(V_1 - V_2) + (V_1 - V_2)\right]$$

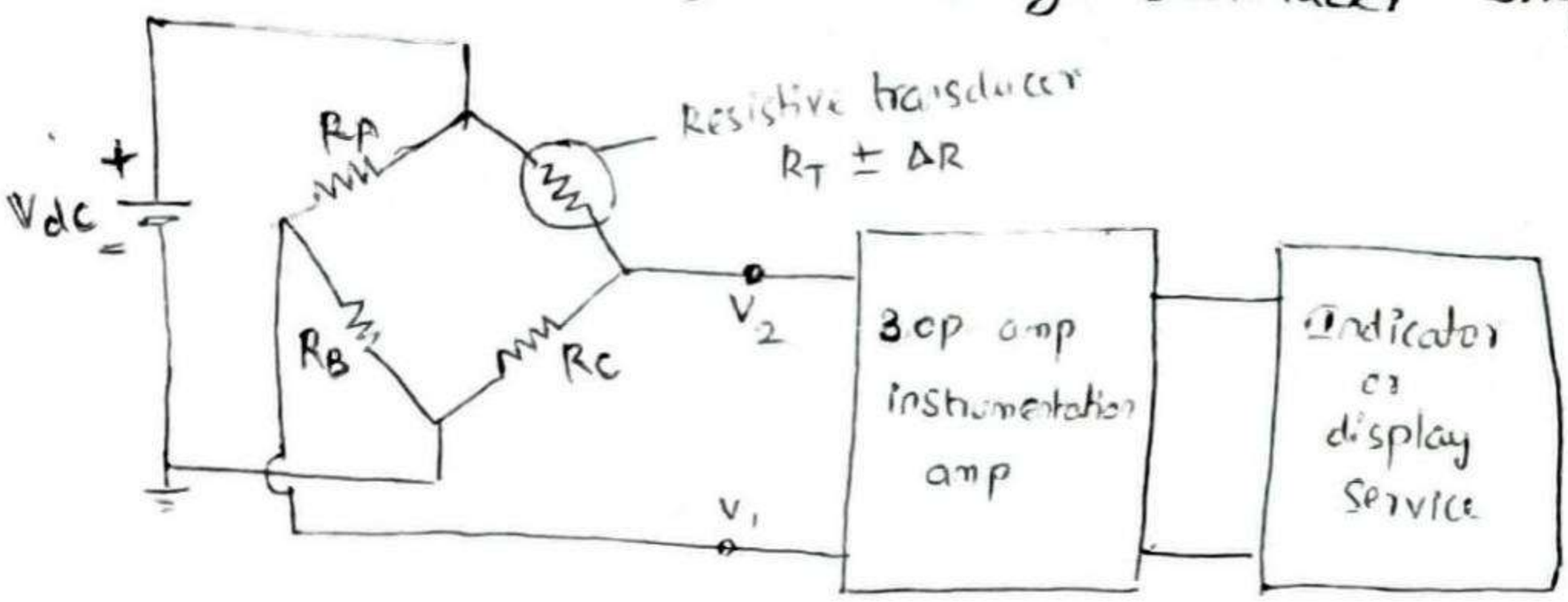
$$\therefore \boxed{V_o = \frac{R_2}{R_1}\left[(V_1 - V_2)\left[2\frac{R'}{R} + 1\right]\right]} \longrightarrow (16)$$

As the above eqn depends upon resistance, if we change the resistance value, the O/P voltage can be controlled.

(3) Instrumentation Amplifier using transducer bridge:

- Ckt use resistive transducer, R_T whose resistance change physical qty to be measured.
- Bridge initially balanced by dc supply voltage V_{dc}, So $V_1 = V_2$

fig IA using transducer bridge



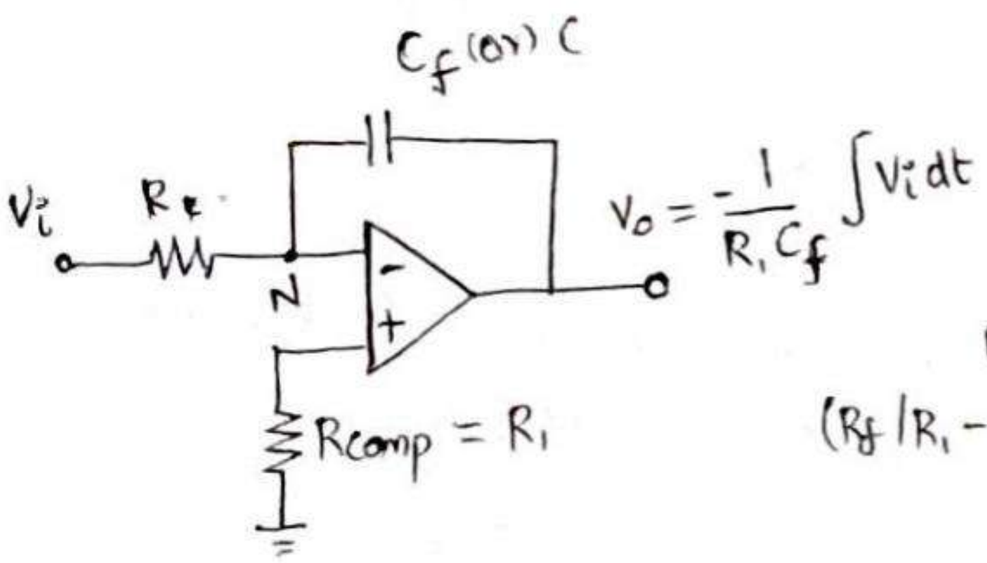
- Phy qty changes, resistance R_T also changes

Applications:

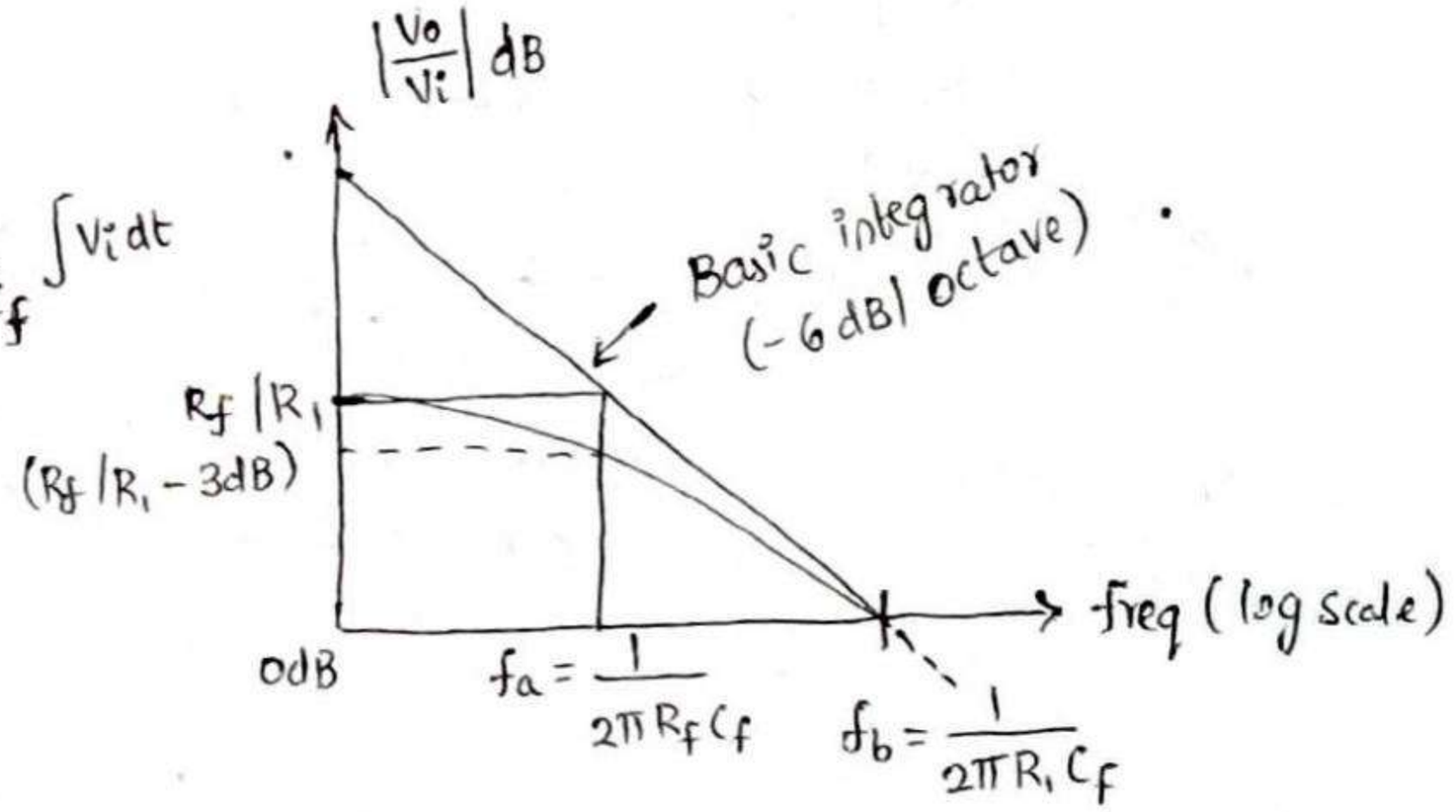
1. Temperature indicator
2. " controller
3. Light intensity meter
4. analog weighing scale
5. measurement of flow of thermal conductivity

IC represents IA are: LH0036, μA725, ICL7605, AD521, AD624
AD624, etc

2.9 INTEGRATOR:



fig(a) Op-amp integrator



fig(b) freq response of a basic & lossy integrator

- One of simplest op-amp ckt that consists of capacitor is integrator
  As name suggests it performs the mathematical function integration
- The nodal eqn at node "N" is analyzed as follows

$$i = \frac{V_i - V_N}{R} = \frac{V_i - 0}{R} = \frac{V_i}{R} \quad \rightarrow (1)$$

Also, $i = C\frac{d}{dt}(V_N - V_o) = C\frac{d}{dt}(-V_o)$ $\rightarrow (2)$

Equating (1) & (2)

$$-C\frac{dV_o}{dt} = \frac{V_i}{R}$$

$$\frac{dV_o}{dt} = -\frac{V_i}{RC}$$

Integrating, $\boxed{V_o = -\frac{1}{RC}\int V_i\, dt}$ $\rightarrow (3)$

- Thus ckt provides o/p voltage proportional to time integral of i/p and RC is the time constant of integrator The negative sign in o/p → inverting indicator
- A simple RC low pass ckt can work as an integrator, when time constant is very large.
- The operation of integrator can be studied in frequency domain

$$V_o(S) = -\frac{1}{SRC} V_i(S) \quad \rightarrow (4)$$

In steady state, put $\boxed{S = j\omega}$, we get

$$V_o(j\omega) = -\frac{1}{j\omega RC} V_i(j\omega) \quad \rightarrow (5)$$

So, the magnitude of gain or integrator Transfer fn. is

$$|A| = \left|\frac{V_o(j\omega)}{V_i(j\omega)}\right| = \left|-\frac{1}{j\omega RC}\right| = \frac{1}{\omega RC} \quad \rightarrow (6)$$

(a) At $\omega = 0$, magnitude $\rightarrow \infty$

(b) At dc, 'C' → open ckt, no -ve feedback

Integrator doesnot face freq problem as faced in differentiator

Practical Integrator ckt (lossy integrator):

- Integrator gain at low freq can be limited to avoid saturation
- Parallel combination of R and C behaves like practical capacitor
- It dissipates power unlike an ideal capacitor for this reason the ckt is called as "lossy integrator"

Analysis

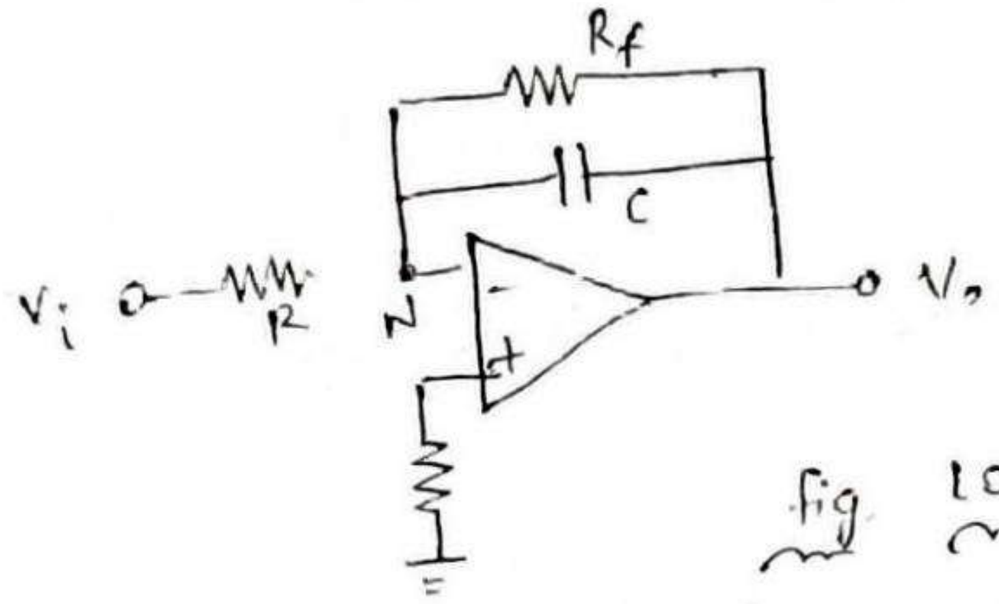


fig lossy integrator ckt

The nodal eqn is

$$\frac{V_i(s)}{R} + sC V_o(s) + \frac{V_o(s)}{R_f} = 0$$

$$\Rightarrow V_o(s) = -\frac{V_i(s)}{R} - sC V_o(s)$$

$$V_o(s)\left[sC + \frac{1}{R_f}\right] = -\frac{1}{R} V_i(s)$$

$$V_o(s)\left(\frac{R_f sC + 1}{R_f}\right) = -\frac{1}{R} V_i(s)$$

$$V_o(s) = \frac{-R_f V_i(s)}{RR_f sC + R} = \frac{-R_f V_i(s)}{R_f[RsC + R/R_f]}$$

$$\therefore \boxed{V_o(s) = -\frac{1}{sCR + R/R_f} \cdot V_i(s)}$$

$$\Rightarrow |A| = \left|\frac{V_o}{V_i}\right| = \frac{1}{\sqrt{\omega^2 R^2 C^2 + R^2/R_f^2}}$$

2. DIFFERENTIATOR:

- One of the simplest of Op-amp ckt that contain capacitor is the differentiating amplifier, or differentiator As name suggests it perform mathematical operation "differentiation", i.e o/p waveform is derivative of i/p waveform

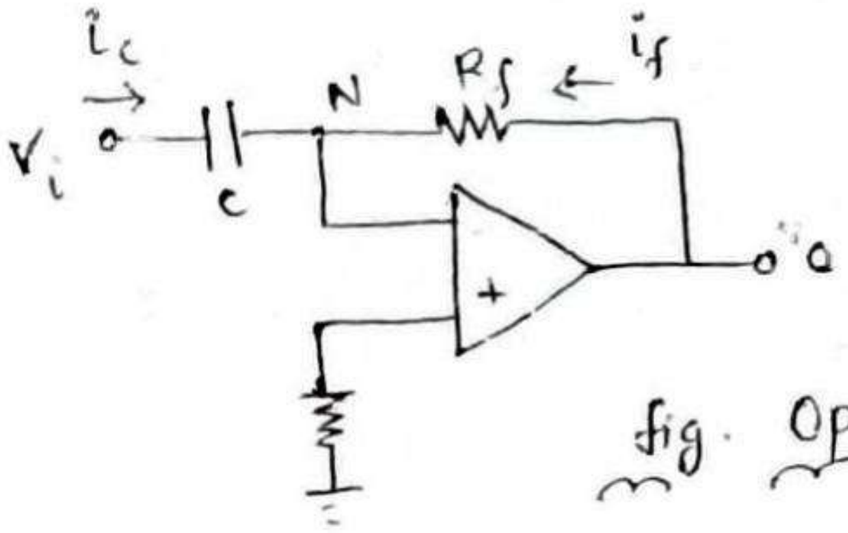


fig. Op-amp differentiator

Analysis:

- The node 'N' is at virtual ground potential i.e $V_N = 0$
- The current through capacitor, $i_c = C \frac{d}{dt}(V_i - V_N)$

$$= C \frac{d}{dt}(V_i - 0)$$

$$\boxed{i = C \frac{dV_i}{dt}} \rightarrow (1)$$

- The current through feedback resistor is, $i = \frac{V_N - V_o}{R_f} = \frac{0 - V_o}{R_f}$

$$\therefore \boxed{i = \frac{-V_o}{R_f}} \rightarrow (2)$$

Equating both current (1) & (2)

$$-\frac{V_o}{R_f} = C \frac{dV_i}{dt}$$

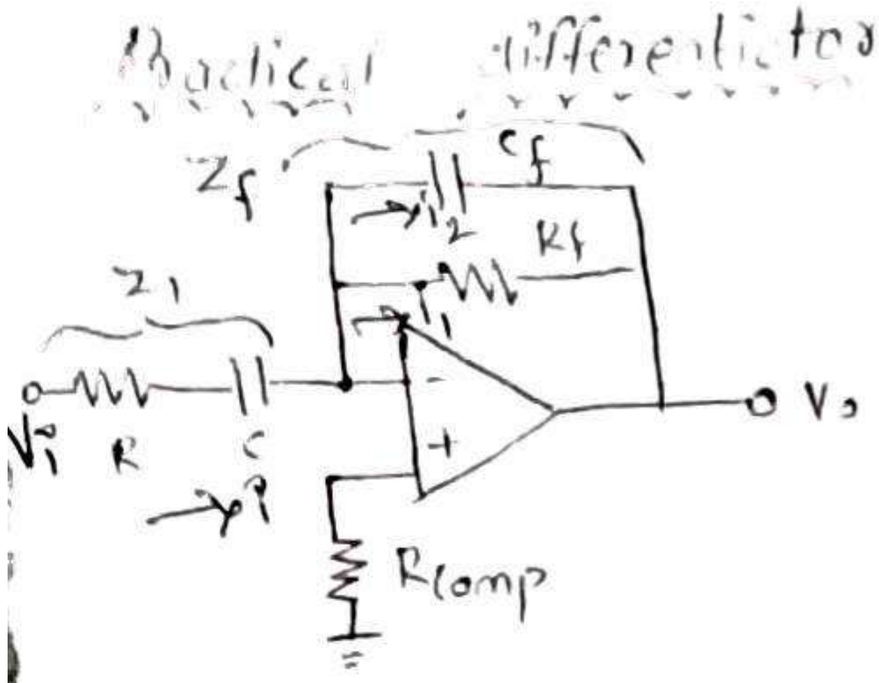
$$\Rightarrow \boxed{V_o = -R_f C \frac{dV_i}{dt}} \rightarrow (3)$$

- Thus o/p voltage V_o is constant $(-R_f C)$ times the derivative of i/p voltage V_i and the ckt is called as "differentiator".
- "−" sign → 180° phase shift of the o/p waveform V_o
- Phase equivalent of eqn. (3) is $V_o(s) = -R_f C V_i(s) s$
- Freq response is $|A| = f/f_a$, where $f_a = \frac{1}{2\pi R_f C}$

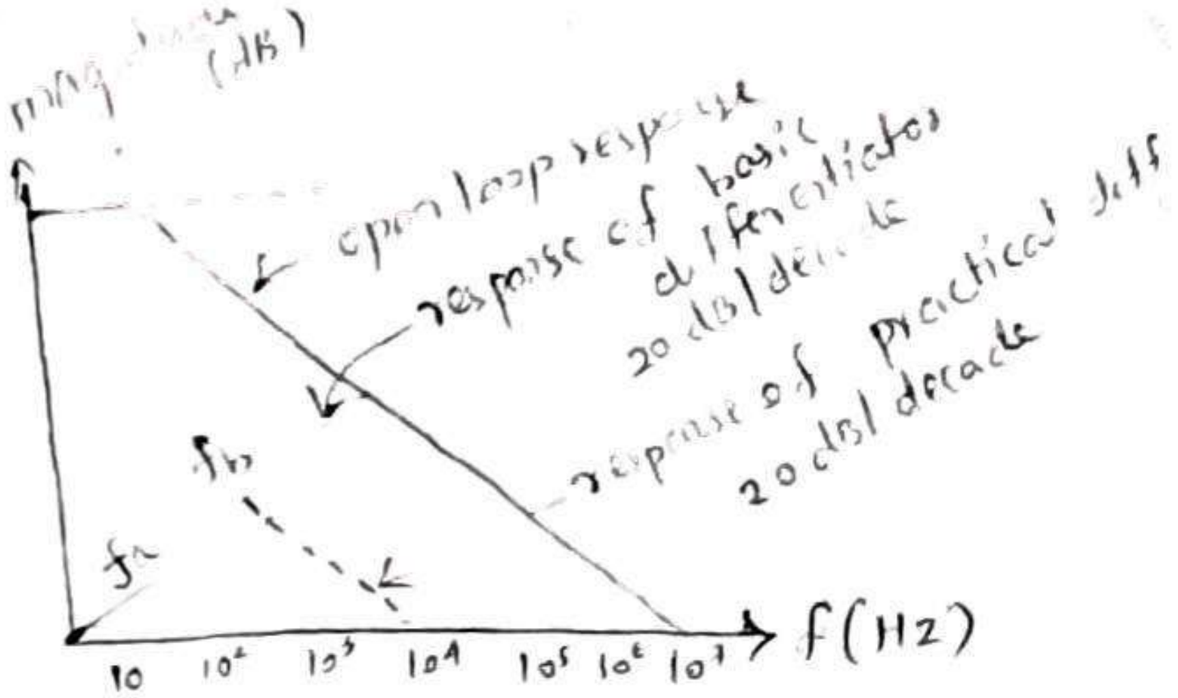
Put $S = j\omega$ & magnitude can be return as

$$|A| = \left|\frac{V_o}{V_i}\right| = |-j\omega R_f C| = \omega R_f C \rightarrow (4)$$

Practical differentiator



(a) practical differentiator



(b) freq response

- PD eliminates problem of instability & high freq noise
- The TF for the ckt is

$$\frac{V_o(s)}{V_i(s)} = \frac{-Z_f}{Z_1} = -\frac{sR_f C}{(1+sR_f C_f)(1+sCR)}$$

For $\boxed{C_f R_f = CR}$, we get $\Rightarrow$ $\frac{V_o(s)}{V_i(s)} = -\frac{sRC}{(1+sRC)^2}$

$$= -\frac{sRC}{(1+jf/f_h)^2} \longrightarrow (5)$$

where, $f_h = \frac{1}{2\pi RC}$

- A resistance R_{comp} is normally connected to (+) i/p terminal to compensate i/p bias ckt
- A good differentiator may be designed as per below :-
  (a) choose f_a = highest freq of i/p signal
  (b) choose f_b = 10 f_a (say) & calculate values of R and C_f
  So $RC = R_f C_f$

LOGIARTHMIC AMPLIFIER & ANTILOG AMPLIFIER

Logarithmic amplifier [Transdiode configuration]

Practical applications of logarithmic amplifier are signal mixing, to find RMS value, Square value, etc of signals

The fundamental log-amp ckt is shown.

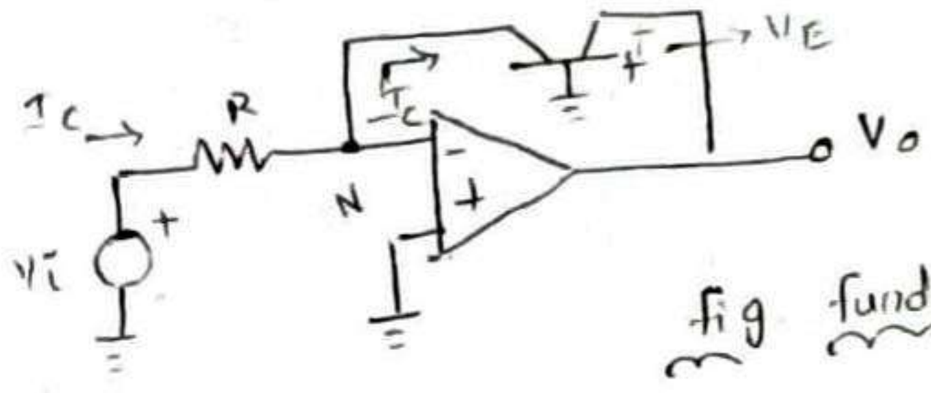


fig fundamental log-amp

. Here a grounded base transistor is in feedback path
. Collector is at virtual ground I/p current is equal to I_C

i e $I_i = I_C$ → ①

. Collector current is given as

$$I_C = I_S \left(e^{V_{BE}/V_t} - 1 \right) \quad \text{where } \boxed{V_t = \frac{KT}{q}} \quad \rightarrow ②$$

I_S → emitter saturation current
K → Boltzmann's constant
T → absolute temperature (in k)

. Since exponential term is far greater than 1, eqn ② becomes

$$I_C \simeq I_S e^{V_{BE}/V_t} \rightarrow ③$$

. Here the base voltage becomes zero, hence $V_{BE} \Rightarrow V_E$

$$I_C \simeq I_S e^{V_E/V_t} \rightarrow ④$$

. Apply KCL at node,

$$I_i = \frac{V_i - V_N}{R} = \frac{V_i - 0}{R} = \frac{V_i}{R} \rightarrow ⑤$$

Equating ③ & ④

$$\Rightarrow \frac{V_i}{R} = I_S e^{V_E/V_t}$$

$$\frac{V_i}{I_S R} = e^{V_E/V_t} \rightarrow ⑤$$

Taking log on both sides,

$$\ln\left(\frac{V_i}{I_{SR}}\right) = \ln e^{V_E/V_t} = V_E/V_t \longrightarrow (7)$$

Therefore, $V_E = V_t \ln\left(\frac{V_i}{I_{SR}}\right) \longrightarrow (8)$

Wkt, the magnitude of V_o & V_E are same but there is a 180° phase shift b/w them. Thus, $\boxed{V_o = -V_E}$

Then $V_o = -V_t \ln\left(\frac{V_i}{I_{SR}}\right) \longrightarrow (9)$

$$\text{Op voltage is } \boxed{V_o = -\frac{kT}{q} \ln\left(\frac{V_i}{V_{ref}}\right)} \longrightarrow (10) \quad (I_{SR} = V_{ref})$$

Problem Identification:

- This ckt has a problem 'I_s' varies from transistor to transistor and with temperature
- A stable V_{ref} can't be obtained.
- This is eliminated by the below ckt, temperature compensation Log-amp ckt

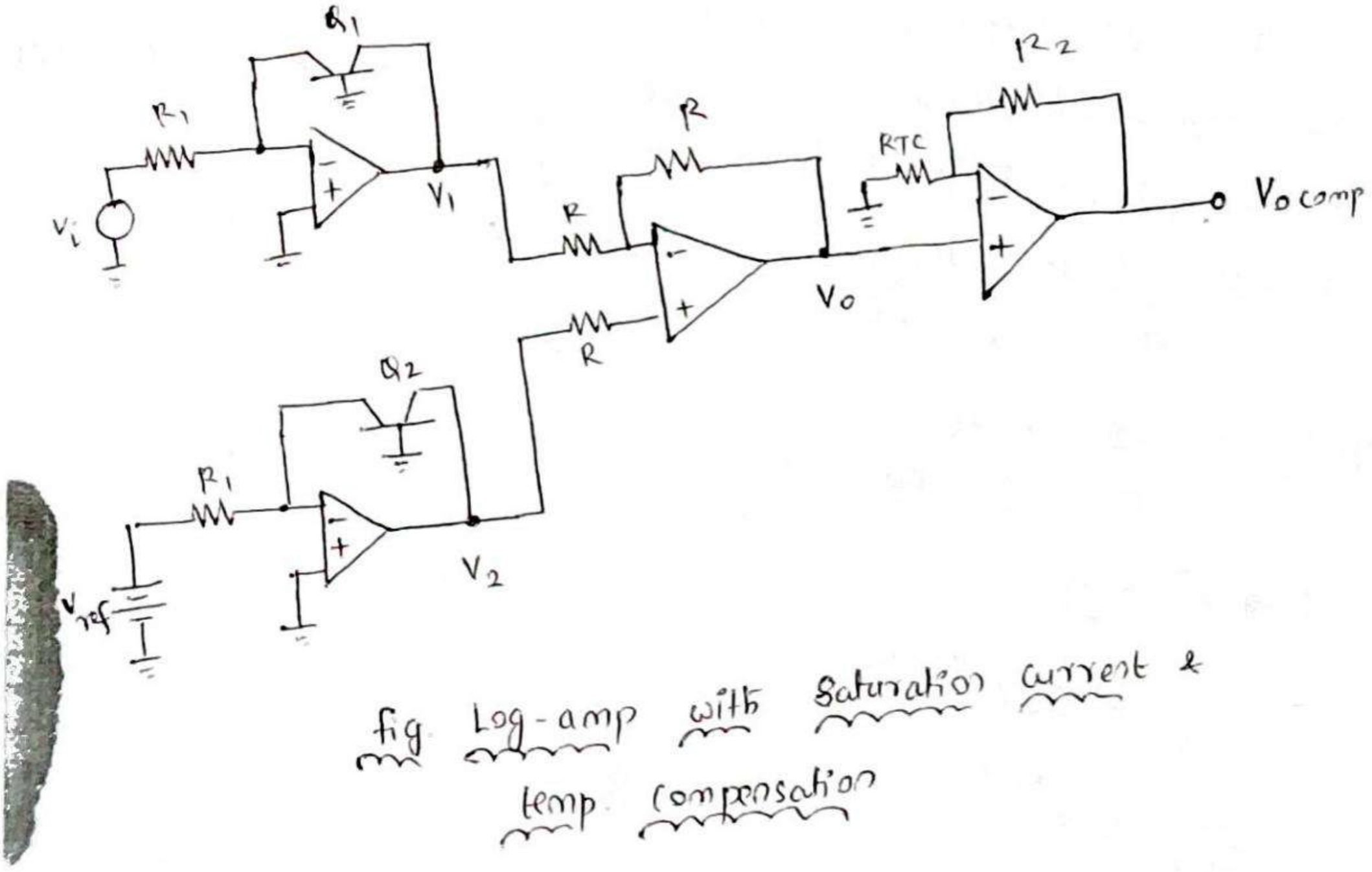


fig Log-amp with Saturation current & temp compensation

Here $V_1 = -V_t \ln\left(V_i / I_S R_1\right)$ from eqn (4) → (11)

Also, $V_2 = -V_t \ln\left(\frac{V_{ref}}{I_S R_1}\right)$ → (12)

WKT $V_o = V_2 - V_1$

$= -V_t \ln\left(\frac{V_{ref}}{I_S R_1}\right) + V_t \ln\left(\frac{V_i}{I_S R_1}\right)$

$= +V_t \left[-\ln\left(\frac{V_{ref}}{I_S R_1}\right) + \ln\left(\frac{V_i}{I_S R_1}\right)\right] = +V_t \ln \frac{\left(\frac{V_i}{I_S R_1}\right)}{\left(\frac{V_{ref}}{I_S R_1}\right)}$

$= -V_t \ln \frac{V_{ref} / I_S R_1}{V_i / I_S R_1}$

$\therefore \boxed{V_o = +V_t \ln\left(\frac{V_i}{V_{ref}}\right)}$ → (13) where, $V_t = \frac{kT}{q}$

Now o/p voltage of the ckt is,

$V_{o\,comp} = \left(1 + \frac{R_f}{R}\right) V_i$ (by non-inverting amp)

$= \left(1 + \frac{R_2}{R_{TC}}\right) V_o$

$\boxed{V_{o\,comp} = +\left(1 + \frac{R_2}{R_{TC}}\right) V_t \ln\left(\frac{V_i}{V_{ref}}\right)}$ → (14)

R_{TC} → temp. sensitive resistance

When R_{TC} is chosen appropriate to V_t, the o/p voltage can be controlled stable.

(b) Antilogarithmic amplifier

- The ckt shown is antilog amp for which i/p V_i is fed into temperature compensating voltage divider R_2 & R_{TC} and then to base of Q_2.
- o/p V_o is fed back to inverting i/p of A_1 through R_1

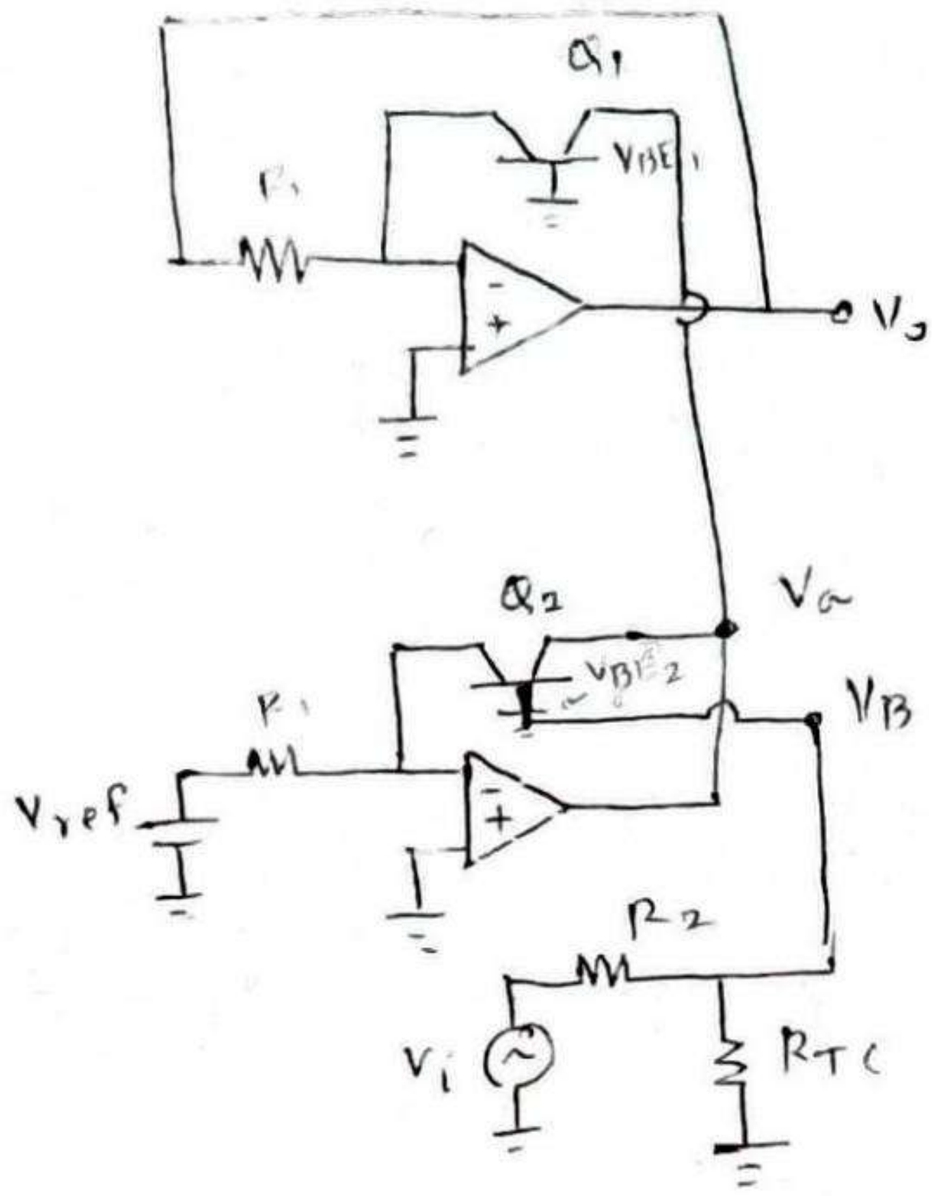


fig analog amp

Apply KVL to Q_2

$$V_B + V_{BE_2} = V_{E_2} \rightarrow (1)$$

Here, $V_a = V_{E_2}$

$$(1) \Rightarrow V_B + V_{BE_2} = V_a \rightarrow (2)$$

We have find these 3 voltages and they are as follows:

$$V_B = \frac{V_i R_{TC}}{R_2 + R_{TC}} \rightarrow (3)$$

$$V_{BE_2} = -V_t \ln \frac{V_{ref}}{I_S R} \rightarrow (4)$$

where $\boxed{V_t = \frac{KT}{q}}$

$$V_a = -V_t \ln \frac{V_o}{I_S R} \rightarrow (5)$$

Sub (3), (4) & (5) in (2)

$$\frac{V_i R_{TC}}{R_2 + R_{TC}} + \left(-V_t \ln \frac{V_{ref}}{I_S R}\right) = -V_t \ln \frac{V_o}{I_S R}$$

$$\frac{V_i R_{TC}}{R_2 + R_{TC}} = V_t \ln \frac{V_{ref}}{I_S R} + V_t \ln \frac{V_o}{I_S R}$$

$$= -V_t \left[-\ln \frac{V_{ref}}{I_S R} + \ln \frac{V_o}{I_S R}\right]$$

$$= -V_t \ln \frac{V_o / I_S R}{V_{ref} / I_S R}$$

$$= -V_t \ln \left(\frac{V_o}{V_{ref}}\right) \rightarrow (6)$$

$\propto$ both sides by 0.4343, to change $\ln \rightarrow \log$

$$\Rightarrow 0.4343 \frac{V_i R_{TC}}{R_2 + R_{TC}} = -V_t \; 0.4343 \ln\left(\frac{V_o}{V_{ref}}\right)$$

$$\Rightarrow 0.4343 \frac{V_i R_{TC}}{R_2 + R_{TC}} = -V_t \log_{10}\left(\frac{V_o}{V_{ref}}\right)$$

$$\Rightarrow -\frac{1}{V_t} 0.4343 \frac{V_i R_{TC}}{R_2 + R_{TC}} = \log_{10}\left(\frac{V_o}{V_{ref}}\right) \longrightarrow (7)$$

Substitute $K' = \frac{1}{V_t} 0.4343 \frac{R_{TC}}{R_2 + R_{TC}}$ in (7)

$$\Rightarrow -K' V_i = \log_{10}\left(\frac{V_o}{V_{ref}}\right) \longrightarrow (8)$$

Take antilog on both sides

$$\Rightarrow 10^{-K' V_i} = \frac{V_o}{V_{ref}}$$

$$\therefore \boxed{V_o = V_{ref}\, 10^{-K' V_i}} \longrightarrow (9)$$

- Therefore increase in i/p by 1V cause o/p to decrease by decade.

2.12 COMPARATORS:

- Comparator is a ckt which compares i/p signal voltage of an op-amp with reference voltage at other i/p of op-amp
- It is open-loop op-amp with o/p $\pm V_{sat}$ ($= V_{cc}$)

Two types:

(a) inverting comparator
(b) non-inverting comparator

(a) non-inverting comparator

- V_{ref} is applied to '−' terminal.
- V_i is applied to '+' terminal
- o/p voltage V_o is at $-V_{sat}$ for $V_i < V_{ref}$

× both sides by 0.4343, to change $\ln \rightarrow \log$

$$\Rightarrow 0.4343 \frac{V_i R_{TC}}{R_2 + R_{TC}} = -V_t \; 0.4343 \ln\left(\frac{V_o}{V_{ref}}\right)$$

$$\Rightarrow 0.4343 \frac{V_i R_{TC}}{R_2 + R_{TC}} = -V_t \log_{10}\left(\frac{V_o}{V_{ref}}\right)$$

$$\Rightarrow -\frac{1}{V_t} 0.4343 \frac{V_i R_{TC}}{R_2 + R_{TC}} = \log_{10}\left(\frac{V_o}{V_{ref}}\right) \longrightarrow (7)$$

Substitute $K' = \frac{1}{V_t} 0.4343 \frac{R_{TC}}{R_2 + R_{TC}}$ in (7)

$$\Rightarrow -K' V_i = \log_{10}\left(\frac{V_o}{V_{ref}}\right) \longrightarrow (8)$$

Take antilog on both sides

$$\Rightarrow 10^{-K' V_i} = \frac{V_o}{V_{ref}}$$

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(a) non-inverting comparator:

- V_{ref} is applied to '−' terminal.
- V_i is applied to '+' terminal
- o/p voltage V_o is at $-V_{sat}$ for $V_i < V_{ref}$

Applications:

(1) Zero crossing detector (Sine to Square wave generator)
(2) Window detector
(3) Time marker generator
(4) Phase meter

2.13 SCHMITT TRIGGER:

- Also known as "Regenerative comparator."
- If +ve feedback added to comparator, gain ↑s
- If loop gain $-\beta A_{OL} = 1$, gain with feedback $A_{vf} = \infty$
- This results in abrupt (zero rise time) transition b/w V_o.
- The following fig shows regenerative compartor.

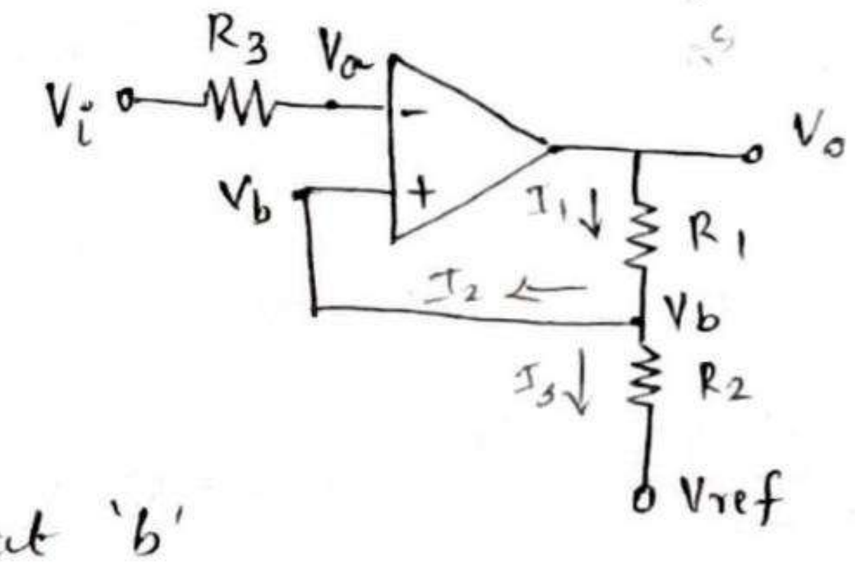


fig schmitt trigger

Apply KCL at 'b'

$$I_1 = I_2 + I_3 \quad \rightarrow (1)$$

By ideal character of op-amp, i/p impedance $= \infty \Rightarrow \frac{V_i}{I_i} = \frac{1}{0}$

$$\therefore I_2 = 0 \quad \rightarrow (2)$$

Eqn (1) $\Rightarrow I_1 = I_3 \quad \rightarrow (3)$

From ckt, $I_1 = \frac{V_b - V_o}{R_1}$, $I_3 = \frac{V_{ref} - V_b}{R_2}$

$$\therefore \frac{V_b - V_o}{R_1} = \frac{V_{ref} - V_b}{R_2}$$

$$\frac{V_b}{R_1} - \frac{V_o}{R_1} = \frac{V_{ref}}{R_2} - \frac{V_b}{R_2}$$

$$\frac{V_b}{R_1} + \frac{V_b}{R_2} = \frac{V_{ref}}{R_2} + \frac{V_o}{R_1}$$

$$\frac{V_b(R_2 + R_1)}{R_1 * R_2} = \frac{V_{ref} R_1 + V_o R_2}{R_1 * R_2}$$

$$\Rightarrow V_b(R_1 \| R_2) = \frac{V_{ref}\ R_1 + V_o\ R_2}{R_1 + R_2}$$

$$\therefore V_b = \frac{V_{ref}\ R_1 + V_o\ R_2}{R_1 + R_2} \rightarrow (4)$$

As per ideal characteristics, op-amp should achieve perfect balance i.e $V_d = 0 \Rightarrow \boxed{V_a = V_b} \rightarrow (5)$

From ckt, $V_a = V_i \Rightarrow V_b = V_i \rightarrow (6)$

(6) in (4) $\Rightarrow$ $$\boxed{V_i = \frac{V_{ref}\ R_1 + V_o . R_2}{R_1 + R_2}} \rightarrow (7)$$

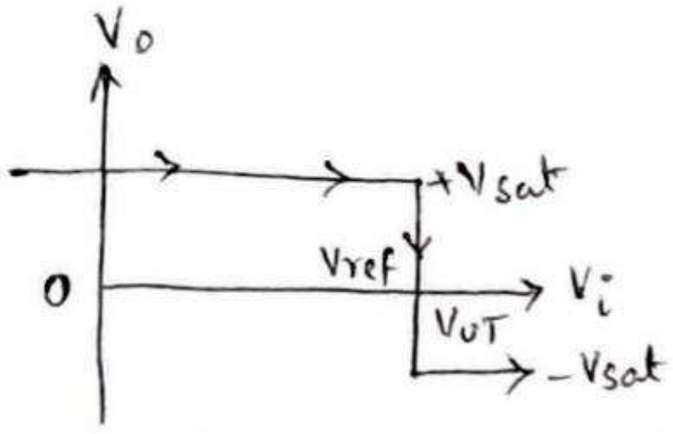
- As i/p voltage is applied to (−) terminal & feedback voltage to (+) terminal, v_i triggers v_o, everytime it exceeds certain voltage levels
- They are called as upper threshold & lower Threshold voltage (V_{UT} & V_{LT})
- Suppose $V_o = +V_{sat}$, then eqn (7) becomes

$$V_{UT} = \frac{V_{ref}\ R_1 + V_{sat}\ R_2}{R_1 + R_2} \rightarrow (8)$$

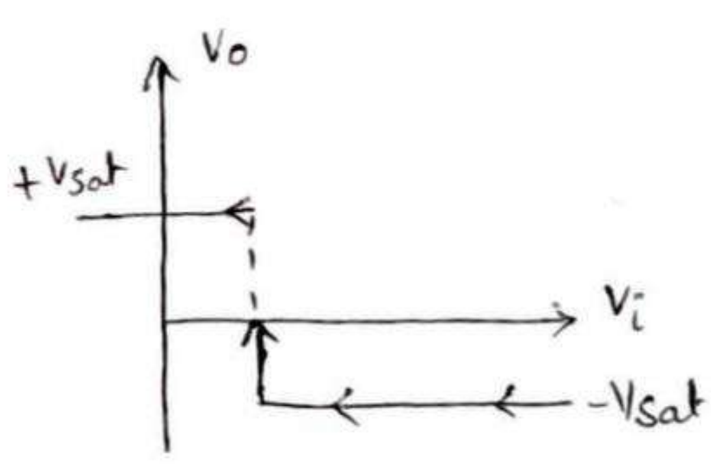
- For $V_o = -V_{sat} \Rightarrow V_{LT} = \frac{V_{ref}\ R_1 - V_{sat}\ R_2}{R_1 + R_2} \rightarrow (9)$
- Now hysteresis voltage is

$$\boxed{V_H = V_{UT} - V_{LT}}$$ (X) problems

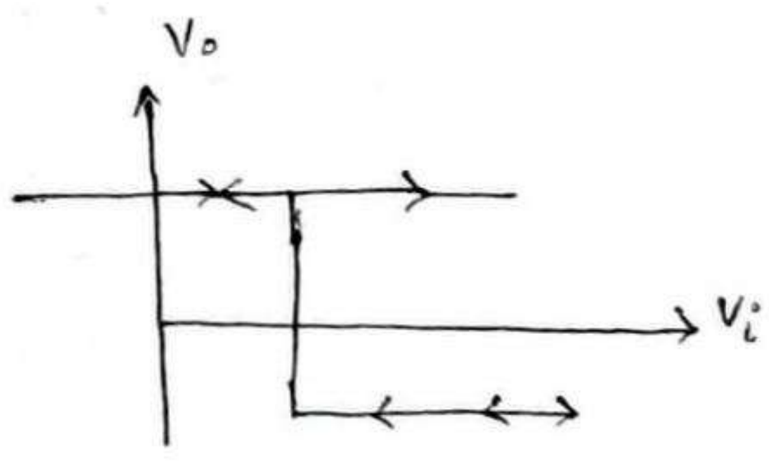
$$= \frac{2 R_2 V_{sat}}{R_1 + R_2}$$



Tranfer characteristics
(a) for V_i increasing



(b) for V_i decreasing



(c) Composite i/p o/p curve

2.14: PRECISION RECTIFIER:

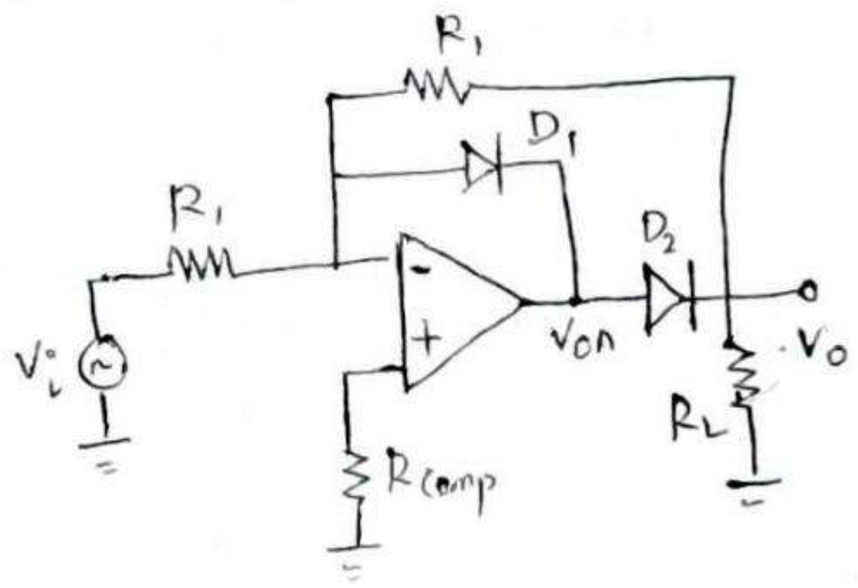
- Major limitation of ordinary diode is that it can't rectify voltage
- A ckt that acts like an ideal diode is designed by placing diode in feedback loop of an OP-amp
- When i/p voltage is higher than V_γ, diode 'D' conducts, whic is called as voltage follower for i/p $V_i > V_\gamma/A_{OL}$ and V_o follows positive half cycle
- When i/p voltage V_i is lesser, then Diode 'D' is OFF,

This ckt is called as precision diode and some applicat are

(a) Half Wave rectifier
(b) Full Wave rectifier
(c) Peak-Value detector
(d) clipper
(e) clamper.

Under precision rectifier, we will discuss half wave & full wave rectifier

(a) Half Wave Rectifier: (HWR)



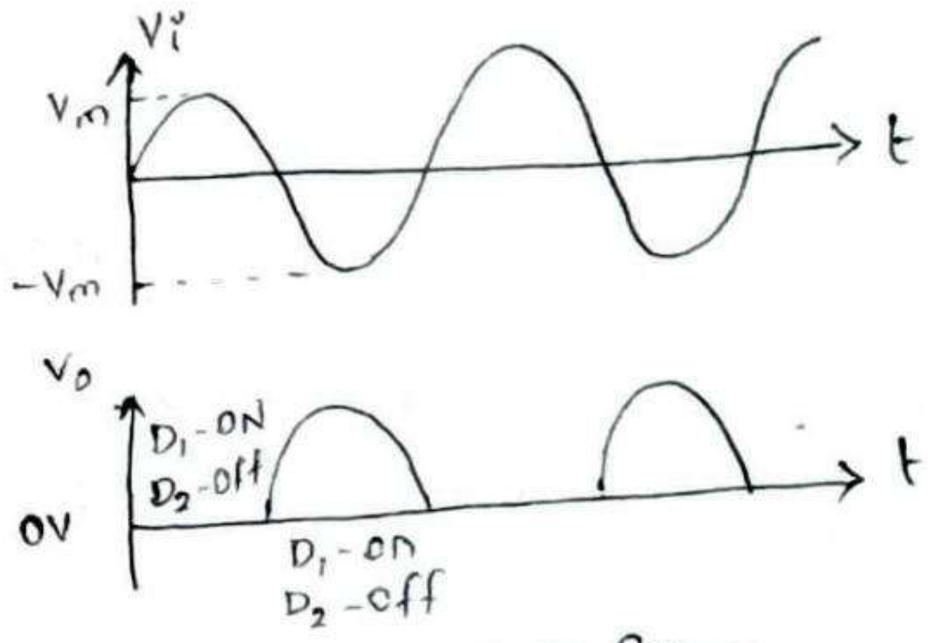


fig (a) Ideal HWR

(b) I/P & o/P waveform

- I/P $V_i \rightarrow$ +ve, diode $D_1 \rightarrow$ conducts, causing V_{oa} to go negative side
  $\therefore D_2 \rightarrow$ reverse biased
- o/p voltage V_o is zero as i/p flows through D_1,
- For $V_i < 0$, diode D_2 conducts and D_1 is off. causing V_{oa} to Positive side $D_2 \rightarrow$ forward biased

- The i/p & o/p waveforms are shown in fig (b)
- The op amp in the ckt must be a high speed op-amp since it alternates b/w open loop & closed loop operations.
- The limitation of this ckt is slew rate.
- The given ckt provides positive o/p if both diodes are reversed, then the input signal gets inverted and provide negative o/p.

(b) Full Wave Rectifier: (FWR)

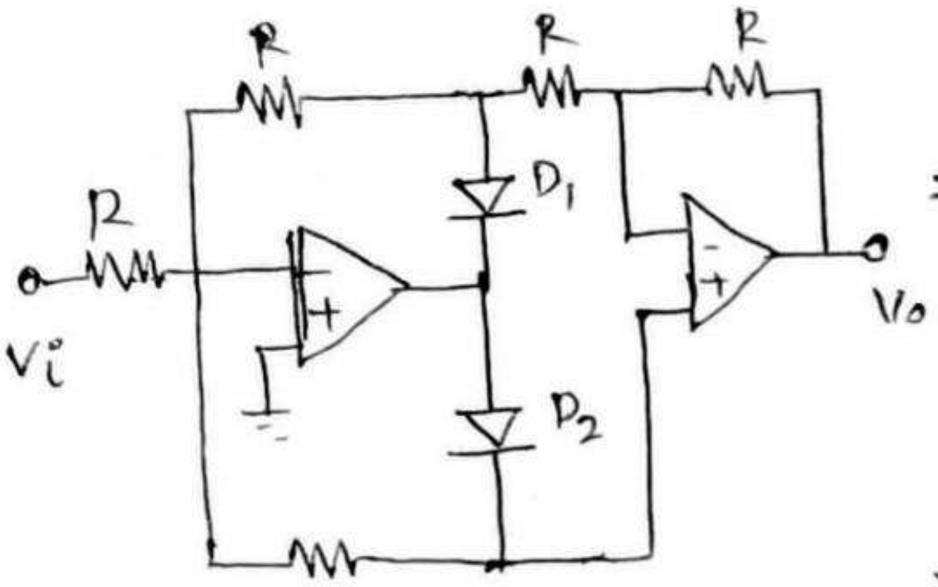


fig (a) Precision FWR

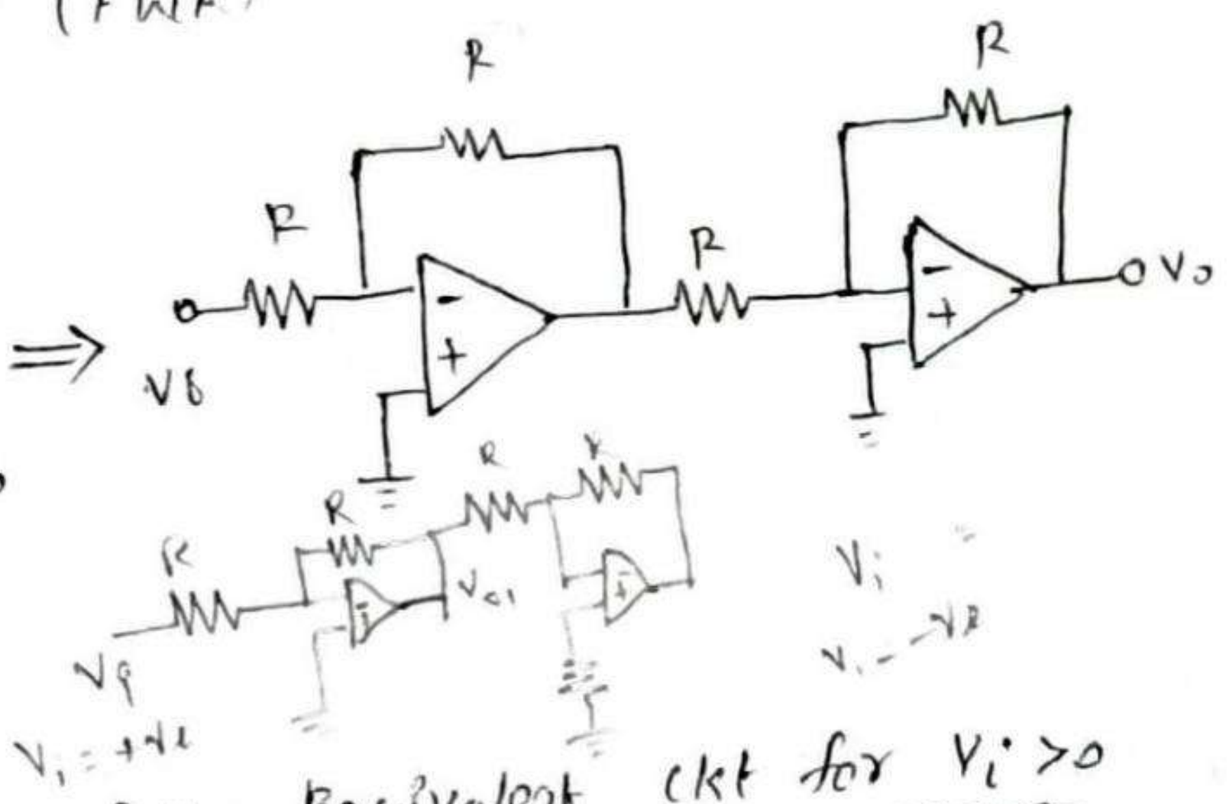


fig (b) Equivalent ckt for $V_i > 0$

- For positive i/p i.e $V_i > 0$, diode D_1 is on, D_2 is off Both op-amp acts as inverter $\therefore$ $\boxed{V_o = V_i}$
- For negative i/p i.e $V_i < 0$, diode D_1 is off, D_2 is on & ith equivalent ckt is as follows.

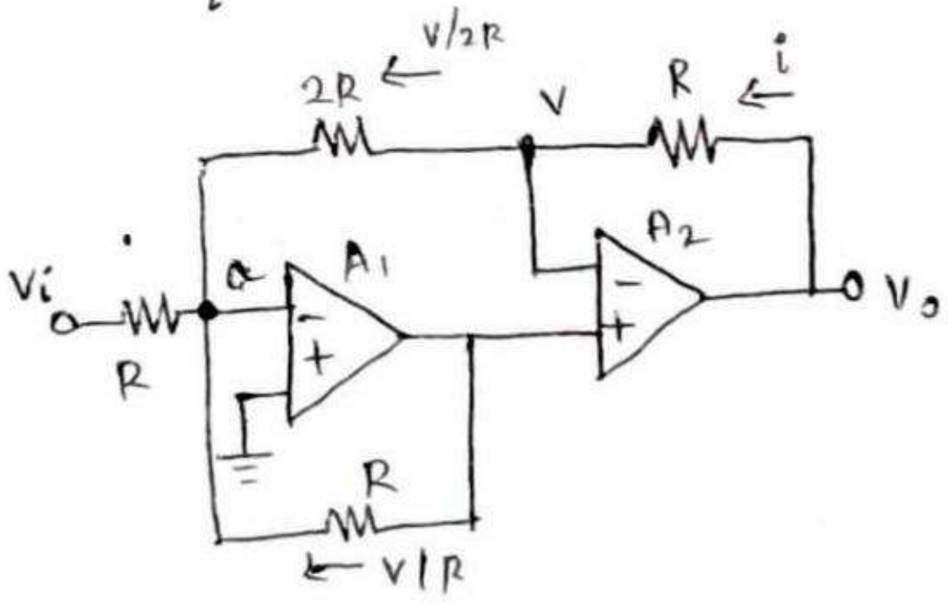


fig (c) ckt for $V_i < 0$

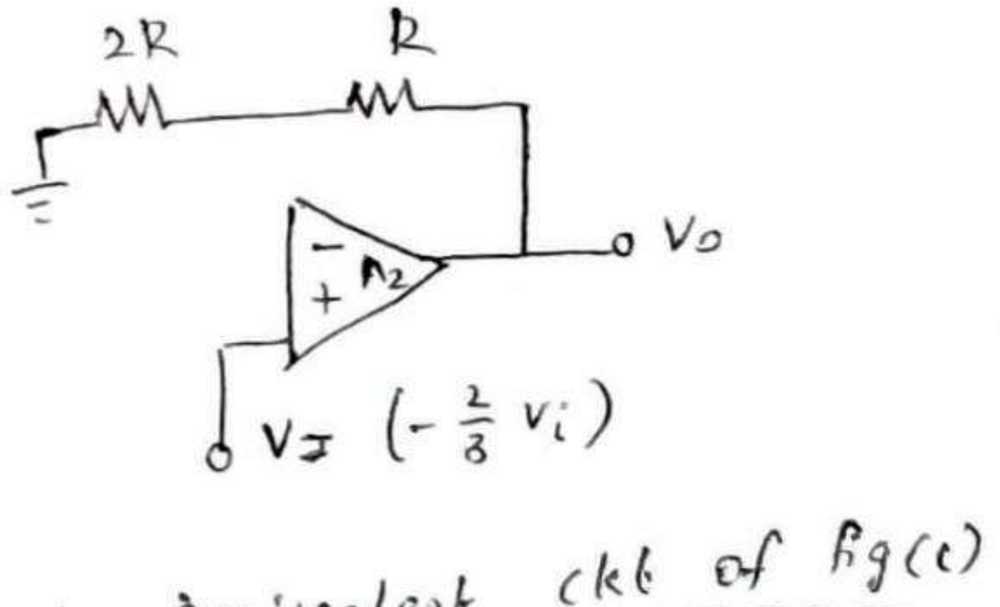


fig (d) equivalent ckt of fig (c)

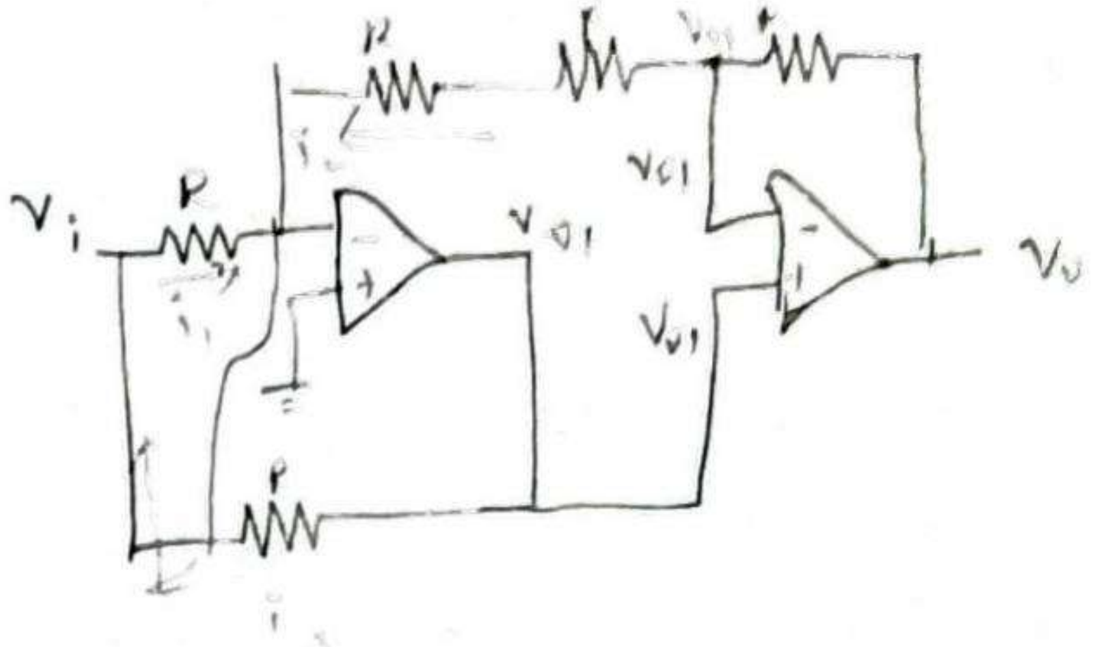
Let i/p voltage n_i is V

KCL at node 'a'

$$\frac{V_i}{R} + \frac{V}{2R} + \frac{V}{R} = 0$$

$$\frac{V_i}{R} + \frac{3V}{2R} = 0$$

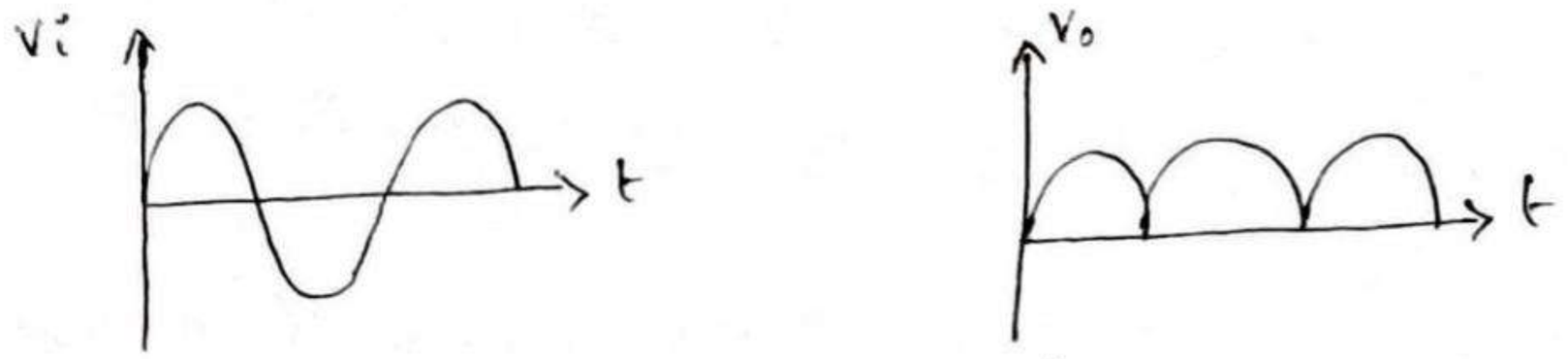
$$\therefore \boxed{V = -\frac{2}{3}V_i}$$



$\therefore$ o/p voltage, $V_o = \left(1 + \frac{R}{2R}\right)\left(-\frac{2}{3}V_i\right) = -V_i$

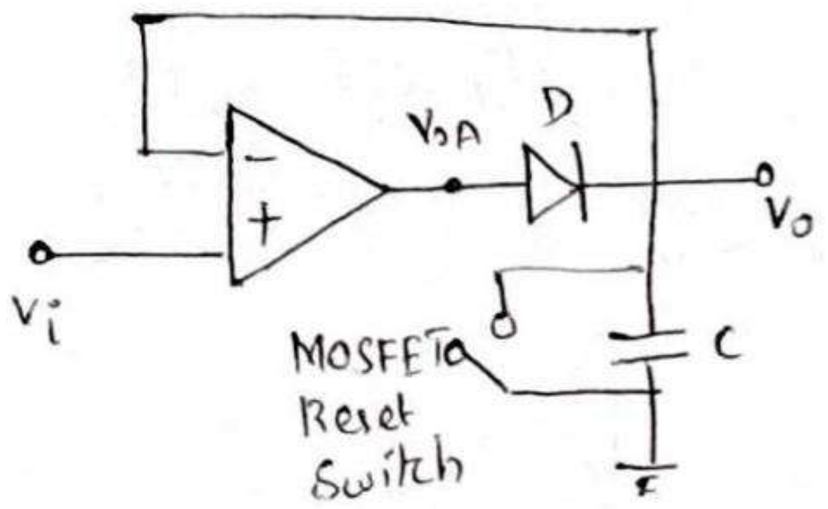
Hence for $V_i < 0$, o/p is negative positive

This ckt is also known as absolute value ckt The i/p & o/p waveform are as follows:

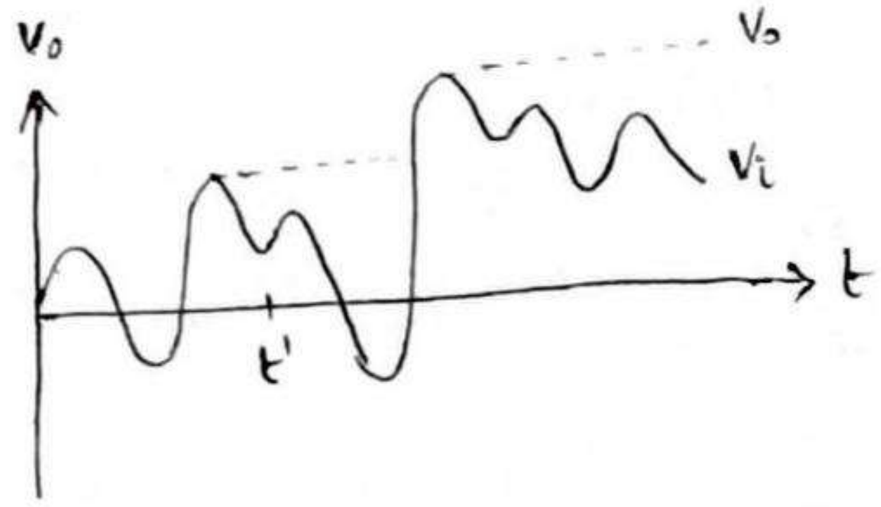


fig(e) I/P & o/p waveform

2.15 PEAK DETECTOR:



(a) positive peak detector



(b) O/P V_o corresponding to arbitary i/p V_i.

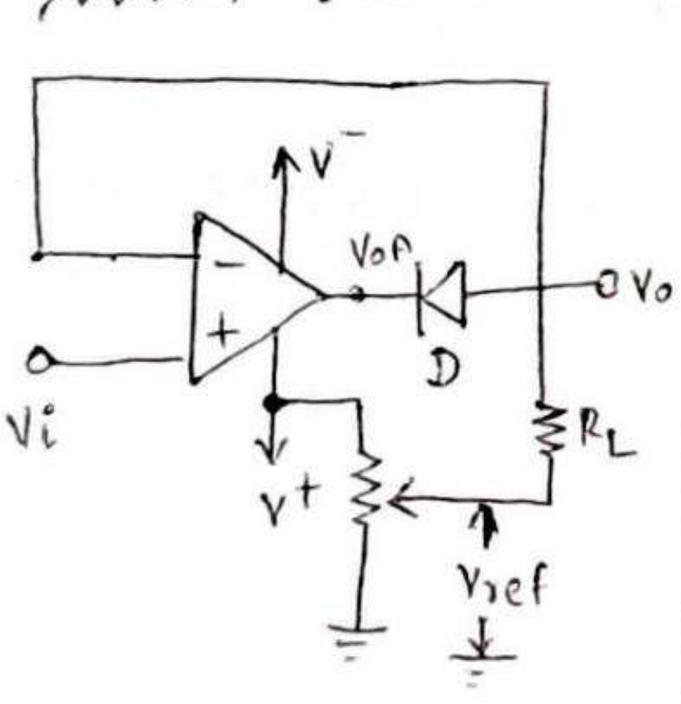
- The fn of a peak detector is to compute the peak value of the i/p
- The ckt follows voltage peaks of a signal & stores highest value on a capacitor
- If a high peak signal value comes along, this new value is stored
- The highest peak value is stored until capacitor is discharged
- When $V_i \geq V_c$, voltage across capacitor; diode 'D' is forward biased & ckt become voltage follower
- o/p V_o follows V_i as long as V_i exceeds V_c
- When $V_i < V_c$, diode is in reverse biased & capacitor hold charge till V_i become greater than V_c ($V_i > V_c$)
- In the given ckt, it is noted that peak at time t' is missed
- Hence MOSFET reset switch is used to reset the ckt, across the capacitor
- Ckt can be modified to hold lowest voltage of a signal, reversing the diode

Application:

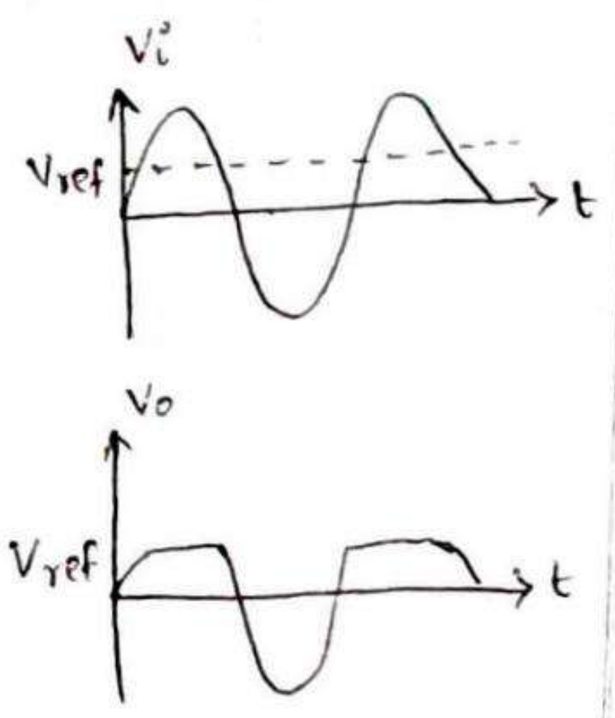
→ In test & measurement instrumentation
→ Amplitude Modulation (AM) communication

2.16 CLIPPER:

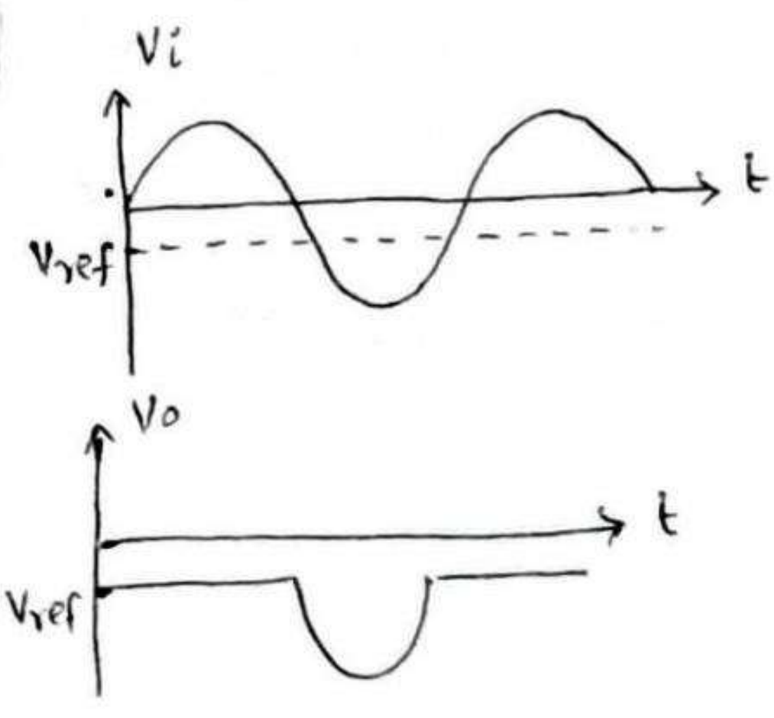
- A precision diode may also be used to clip-off a certain portion of i/p signal to obtain desired o/p waveform



(a) positive clipper

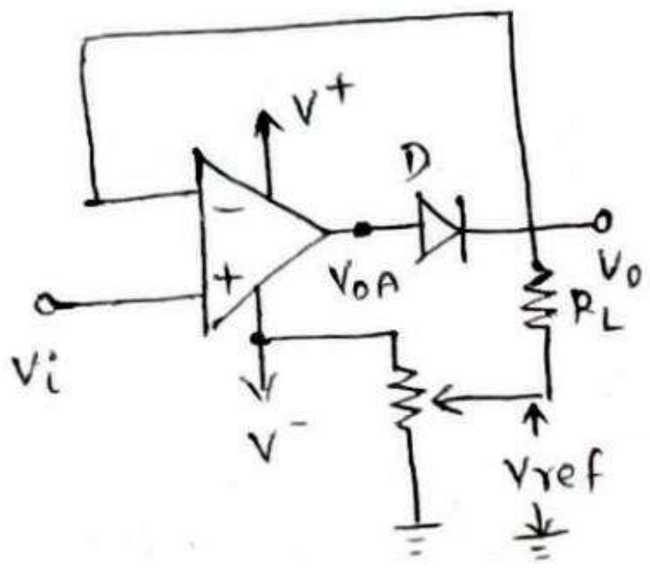


(b) positive V_{ref}

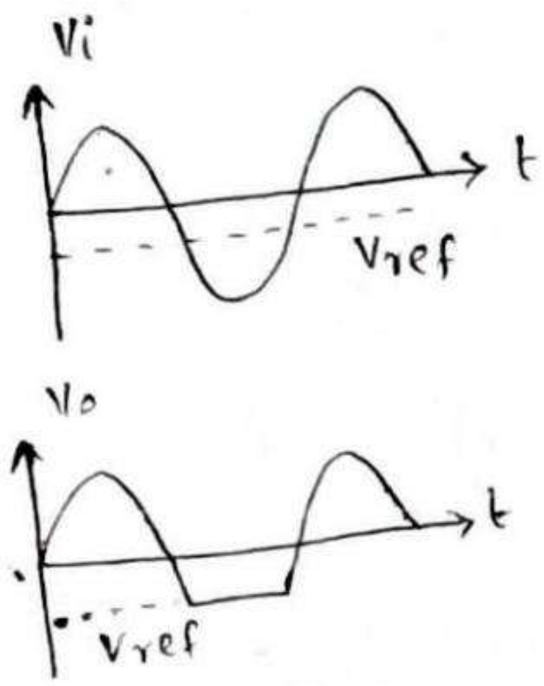


(c) negative V_{ref}

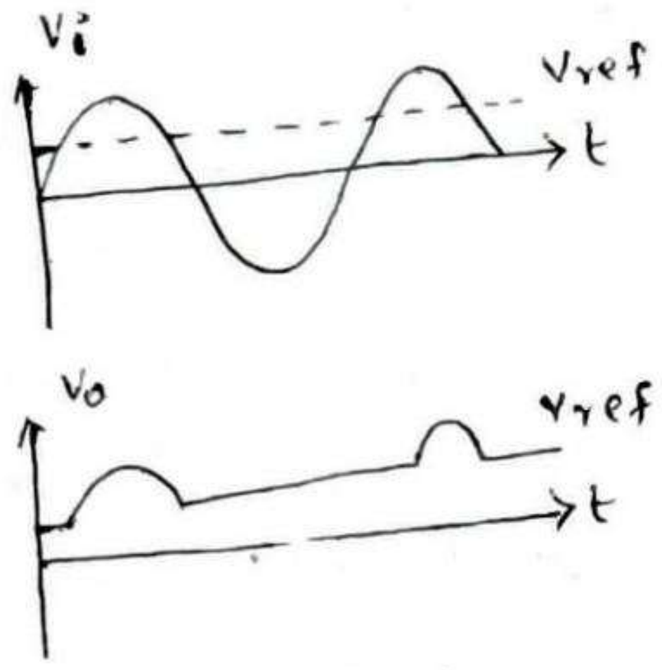
- clipping level is determined by V_{ref} and could be obtained from positive supply voltage V^+
- It can be seen that portion of o/p voltage for $V_o > V_{ref}$ are clipped off
- For i/p voltage, $V_i < V_{ref}$, diode 'D' conducts
- op-amp works as voltage follower, V_o follows V_i, till $V_i \leq V_{ref}$
- When $V_i > V_{ref}$, V_{OA} is large and will drive 'D' into cut off
- If V_{ref} is negative, then entire o/p waveform above V_{ref} will get clipped off as shown as follows: in fig a, b, c



fig(d) negative clipper



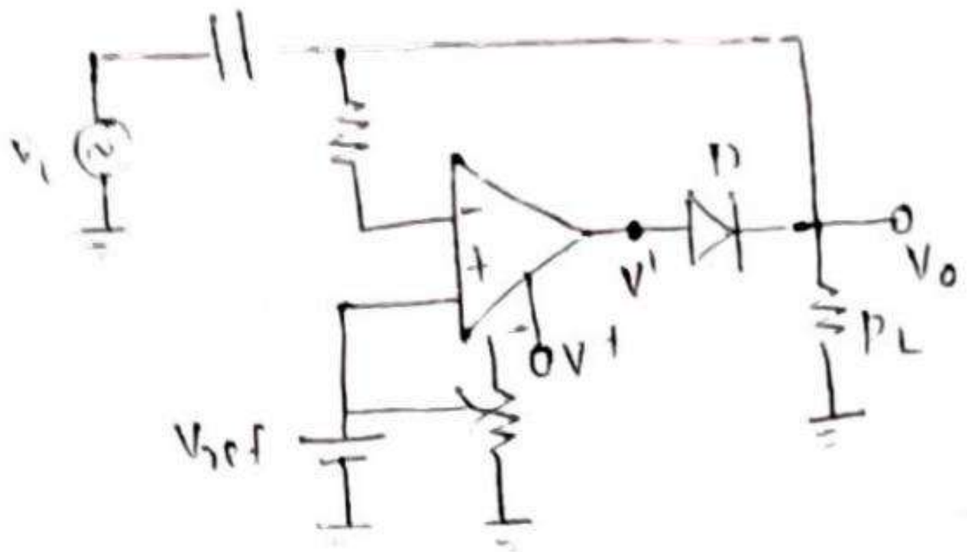
(e) negative Vref



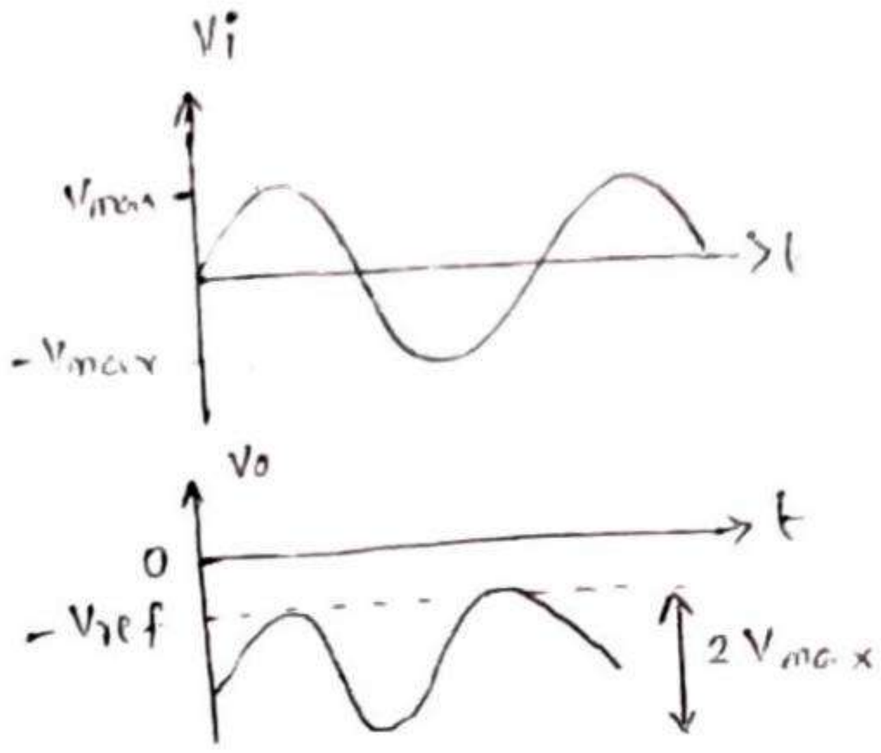
(f) positive Vref

- Positive clipper of fig (a) can be easily converted into a negative clipper by simply reversing diode 'D' and changing polarity of the reference voltage V_{ref}
- Negative clipper clips off negative parts of i/p signal below V_{ref}
- ckt diagram of negative clipper & the expected waveform is shown in fig (d, e, f)

2.17 CLAMPER:

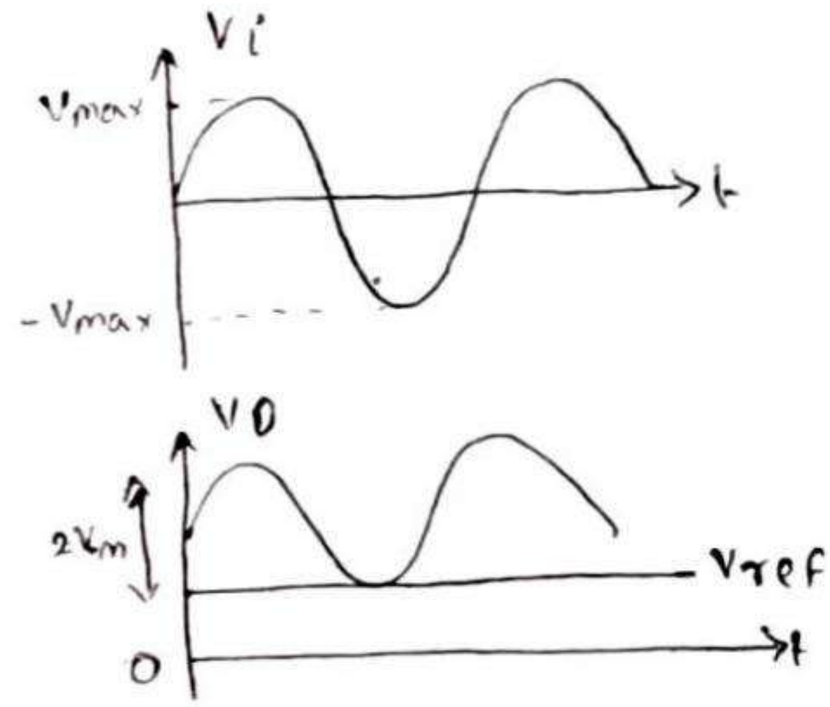


fig(a) peak clamper



(b) waveform for $-V_{ref}$

- clamper is also known as "inserter or restorer"
- ckt is used to add desired dc level to o/p voltage i.e o/p voltage is clamped to desired dc level.
- If clamped dc level is positive, it is positive clamper
- If clamped dc level is negative, it is negative clamper



(c) waveform for $+V_{ref}$

- Positive dc voltage applied at (+) terminal, which clamps peak of i/p waveform. o/p voltage is net result of ac/dc Vi at (-) & (+) terminals
- For positive Vref, V' is positive, Diode 'D' is forward biased
- I/P signal Vi is applied at (-) terminal. During -ve half cycle Diode 'D' conducts, 'capacitor 'c' charge through diode 'D' to negative peak voltage V_{max}.
- During positive half cycle, 'D' is reverse biased & capacitor retains its previous voltage V_m

- The negative peak clamping is obtained by reversing the diode 'D' and using negative reference voltage -Vref
- Resistor R is used for protecting op-amp against excessive discharge current from capacitor 'C' especially when dc voltage supply are switched off

2.18 ACTIVE FILTERS:

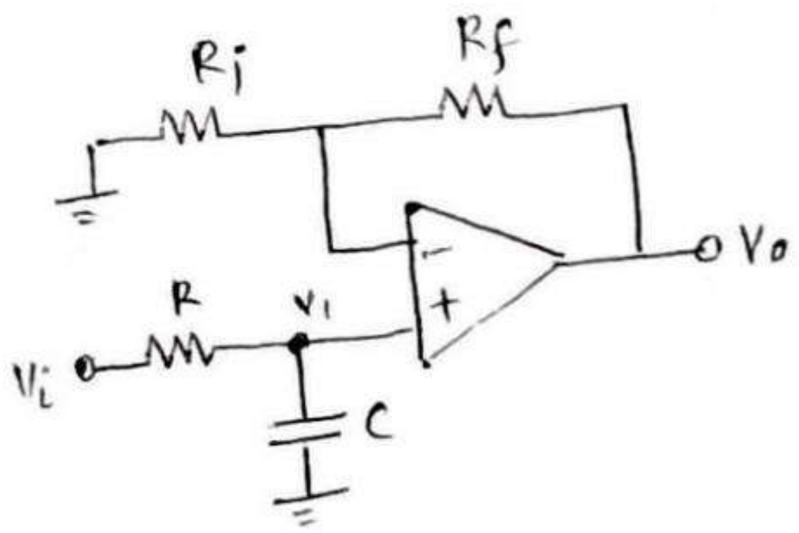
Filters are used in ckt that pass require separation of signals according to their frequencies. They are widely used in communication & signal processing. The 3 configuration of active filters are

1. Low pass filter (LPF)
2. High pass filter (HPF)
3. Band pass filter (BPF)

(1) Low pass filter (LPF):

Active filters may be of different order and types. LPF can be classified as
(a) First order low pass filter
(b) Second order "

(a) First order LPF:



fig(a) First ord LPF & its freq response

As per non-inverting amp gain,

$$V_o(s) = \left(1 + \frac{R_F}{R_i}\right) V_1 \quad \rightarrow (1)$$

To find $V_1(s)$: $V_1(s) = \frac{1/sC}{R + 1/sC} V_i(s)$

$$V_1(s) = \frac{1}{1 + sRC} V_i(s) \quad \rightarrow (2)$$

(2) in (1)

$$V_o(s) = \left(1 + \frac{R_F}{R_i}\right) \frac{V_i(s)}{1 + sRC}$$

$$\frac{V_o(s)}{V_i(s)} = A_0 \frac{1}{1 + sRC} \quad \rightarrow (3)$$

By Laplace transform,

$$H(s) = \frac{V_o(s)}{V_i(s)} = \frac{A_0}{1 + sRC} \quad \rightarrow (4)$$

Let $\omega_h = \frac{1}{RC} \Rightarrow RC = \frac{1}{\omega_h}$

$$\therefore \boxed{H(s) = \frac{A_0}{1 + s/\omega_h} = \frac{A_0 \omega_h}{s + \omega_h}} \quad \rightarrow (5)$$

→ std form of Transfer fn of 1st order LPF

Put $\boxed{s = j\omega}$ in (4)

$$H(j\omega) = \frac{A_0}{1 + j\omega RC}$$

Sub $\boxed{\omega = 2\pi f} \Rightarrow H(j\omega) = \frac{A_0}{1 + j 2\pi f RC} \quad \rightarrow (6)$

Here, $f_h = \frac{1}{2\pi RC}$

$$\therefore H(j\omega) = \frac{A_0}{1 + j(f/f_h)} \quad \rightarrow (7)$$

(i) At very low freq, $f << f_h$ (passband)

$$\boxed{|H(j\omega)| \simeq A_0}$$

(ii) At $f = f_h$

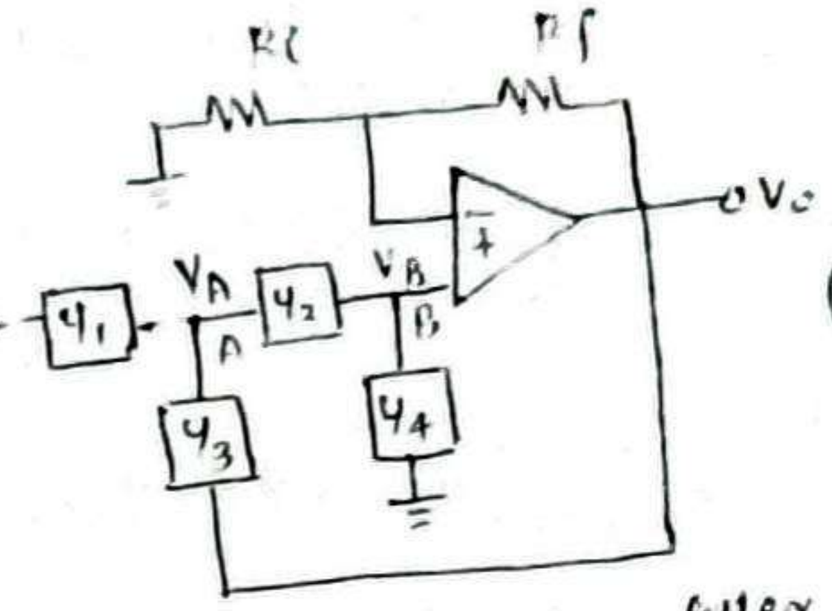
$$\boxed{|H(j\omega)| = \frac{A_0}{\sqrt{2}}}$$ (Cutoff frequency)

(iii) At very high freq, $f >> f_h$ (Stopband)

$$\boxed{|H(j\omega)| << A_0 \simeq 0}$$

(b) Second order Active LPF (Sallen key filter)

- An improved filter response obtained using 2nd order active filter
- It consists of a pair of RC combination and has a roll-off rate of -40dB/decade
- A general 2nd order filter (Sallen-key) is shown in fig(a)



Hint
(Y - admittance & inverse of resistance Y = 1/R)

fig Sallen key filter

- It can be used for analysing LPF & HPF

The op-amp is connected as non-inverting amp, hence

$$V_o = \left(1 + \frac{R_f}{R_i}\right) V_B = A_o V_B \quad \rightarrow ① \quad \rightarrow ②$$

$$\Rightarrow V_B = V_o / A_o$$

Node 'A' → apply KCL

$$(V_A - V_i) Y_1 + (V_A - V_B) Y_2 + (V_A - V_o) Y_3 = 0$$

$$V_A Y_1 - V_i Y_1 + V_A Y_2 - V_B Y_2 + V_A Y_3 - V_o Y_3 = 0$$

$$V_A (Y_1 + Y_2 + Y_3) - V_i Y_1 - V_B Y_2 - V_o Y_3 = 0$$

$$V_A (Y_1 + Y_2 + Y_3) - V_B Y_2 - V_o Y_3 = V_i Y_1 \quad \rightarrow ③$$

Sub ② in ③

$$V_A (Y_1 + Y_2 + Y_3) - \frac{V_o}{A_o} Y_2 - V_o Y_3 = V_i Y_1 \quad \rightarrow ④$$

KCL at 'B'

$$(V_B - V_A) Y_2 + (V_B - 0) Y_4 = 0$$

$$V_B Y_2 - V_A Y_2 + V_B Y_4 = 0$$

$$V_B (Y_2 + Y_4) - V_A Y_2 = 0$$

$$V_B (Y_2 + Y_4) = V_A Y_2$$

$$\therefore V_A = \frac{V_B (Y_2 + Y_4)}{Y_2} \quad \rightarrow ⑤$$

Sub ② in ⑤

$$V_A = \frac{V_o (Y_2 + Y_4)}{A_o Y_2} \quad \rightarrow ⑥$$

Sub (ii) in (i)

$$V_i Y_1 = \frac{V_o}{A_o}\left(\frac{Y_3+Y_4}{Y_2}\right)(Y_1+Y_2+Y_3) - \frac{V_o}{A_o}Y_2 - V_o Y_3$$

$$= \frac{V_o(Y_3+Y_4)(Y_1+Y_2+Y_3) - V_o Y_2^2 - V_o A_o Y_3 Y_2}{A_o Y_2}$$

$$= \frac{V_o}{A_o Y_2}\left[Y_1Y_2 + Y_2^2 + Y_2Y_3 + Y_1Y_4 + Y_2Y_4 + Y_3Y_4 - Y_2^2 - A_o Y_3 Y_2\right]$$

$$V_i Y_1 = \frac{V_o}{A_o Y_2}\left[Y_1Y_2 + Y_2Y_3(1-A_o) + Y_4(Y_1+Y_2+Y_3)\right]$$

$$\frac{V_o}{V_i} = \frac{A_o Y_1 Y_2}{Y_1Y_2 + Y_2Y_3(1-A_o) + Y_4(Y_1+Y_2+Y_3)} \rightarrow (7)$$

This gain formula for 2nd order active filter

Second order LPF :-

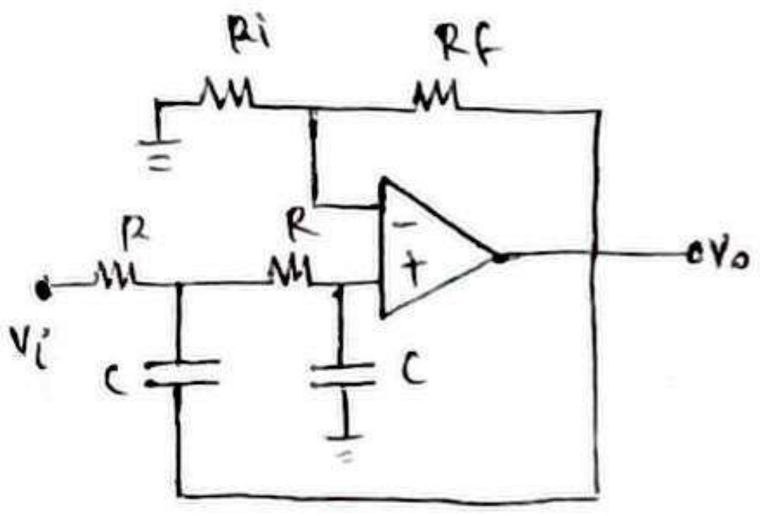


fig 2nd order LPF

Sub $Y_1 = Y_2 = \frac{1}{R}$; $Y_3 = Y_4 = SC$ in (7)

$$\Rightarrow H(S) = \frac{A_o\left(\frac{1}{R}\right)\left(\frac{1}{R}\right)}{\left(\frac{1}{R}\right)\left(\frac{1}{R}\right) + \left(\frac{1}{R}\right)(SC)(1-A_o) + SC\left(\frac{1}{R}+\frac{1}{R}+SC\right)}$$

$$= \frac{A_o/R^2}{\frac{1}{R^2} + \frac{SC}{R}(1-A_o) + SC\left(\frac{2}{R}+SC\right)}$$

Taking LCM

$$H(S) = \frac{A_o/R^2}{\frac{1}{R^2} + \frac{SCR(1-A_o)}{R^2} + SCR\left(\frac{2+SRC}{R^2}\right)}$$

$$= \frac{A_o}{1 + SCR(1-A_o) + SCR(2+SRC)}$$

$$= \frac{A_o}{1 + SCR[1-A_o+2+SRC]}$$

$$\Rightarrow H(s) = \frac{A_0}{1 + SRC(3 - A_0 + SRC)}$$

$$= \frac{A_0}{1 + SRC(3 - A_0) + (SRC)^2} \quad \rightarrow (8)$$

If $S = 0 \Rightarrow H(0) = A_0$

$S = \infty \Rightarrow H(\infty) = 0$

Let $\omega_h = \frac{1}{RC}$ & $\alpha = 3 - A_0$

$RC = \frac{1}{\omega_h}$

where $\alpha \rightarrow$ damping co-efficient
$A_0 \rightarrow$ gain
$\omega_h \rightarrow$ upper cut off frequency in radian/sec

$$H(s) = \frac{A_0}{1 + s\left(\frac{1}{\omega_h}\right)\alpha + \left(\frac{s}{\omega_h}\right)^2} \quad \rightarrow (9)$$

$$H(s) = \frac{A_0}{\left(\frac{s}{\omega_h}\right)^2 + \left(\frac{s}{\omega_h}\right)\alpha + 1} \quad \rightarrow (10)$$

Taking LCM

$$H(s) = \frac{A_0 \cdot \omega_h^2}{s^2 + s\omega_h\alpha + \omega_h^2}$$

Put $\boxed{s = j\omega}$

$$H(j\omega) = \frac{A_0\ \omega_h^2}{(j\omega)^2 + (j\omega)\omega_h\alpha + \omega_h^2}$$

$$= \frac{A_0}{\frac{(j\omega)^2}{\omega_h^2} + \frac{j\omega\omega_h\alpha}{\omega_h^2} + \frac{\omega_h^2}{\omega_h^2}}$$

$$= \frac{A_0}{\frac{-\omega^2}{\omega_h^2} + j\frac{\omega\alpha}{\omega_h} + 1}$$

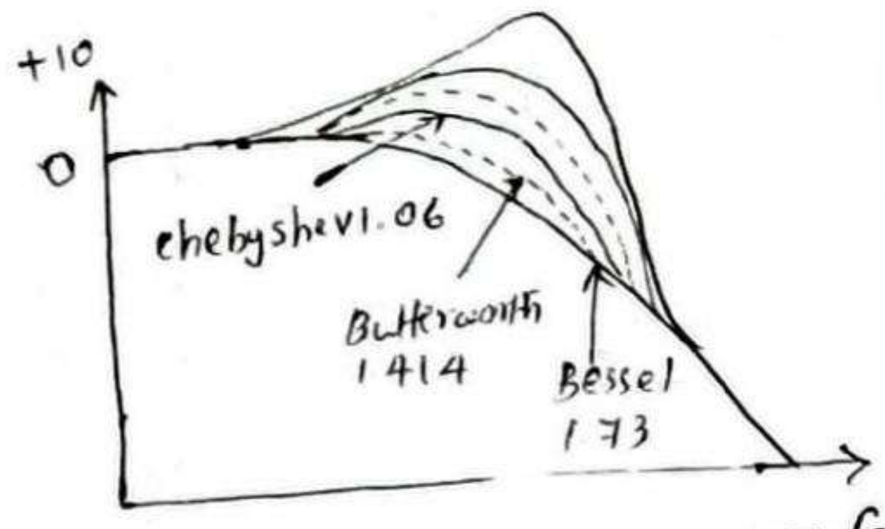


fig. 2nd order LPF response for different damping

Separating Real & imaginary terms,

$$H(j\omega) = \frac{A_0}{\left(1 - \frac{\omega^2}{\omega_h^2}\right) + j\frac{\omega\alpha}{\omega_h}}$$ ← as (a+ib) form

$$\therefore |H(j\omega)| = \frac{A_0}{\sqrt{1 + \left(\frac{\omega^2}{\omega_h^2}\right)^2 - \frac{2\omega^2}{\omega_h^2} + \frac{\omega^2\alpha^2}{\omega_h^2}}} \quad \rightarrow (11)$$

Let $S_n = \frac{S}{\omega_h}$ in eqn (9)

$$\boxed{H(S_n) = \frac{A_0}{1 + S_n\alpha + S_n^2}} \quad \rightarrow (12)$$

For Butterworth filters, [A = 1.414] From fig

Sub 'A' in eqn (11)

$$|H(j\omega)| = \frac{A_0}{\sqrt{1+\left(\frac{\omega}{\omega_h}\right)^4 - \frac{2\omega^2}{\omega_h^2} + \frac{\omega^2}{\omega_h^2}(1.414)^2}}$$

$$= \frac{A_0}{\sqrt{1+\left(\frac{\omega}{\omega_h}\right)^2 - \frac{2\omega^2}{\omega_h^2} + \frac{2\omega^2}{\omega_h^2}}}$$

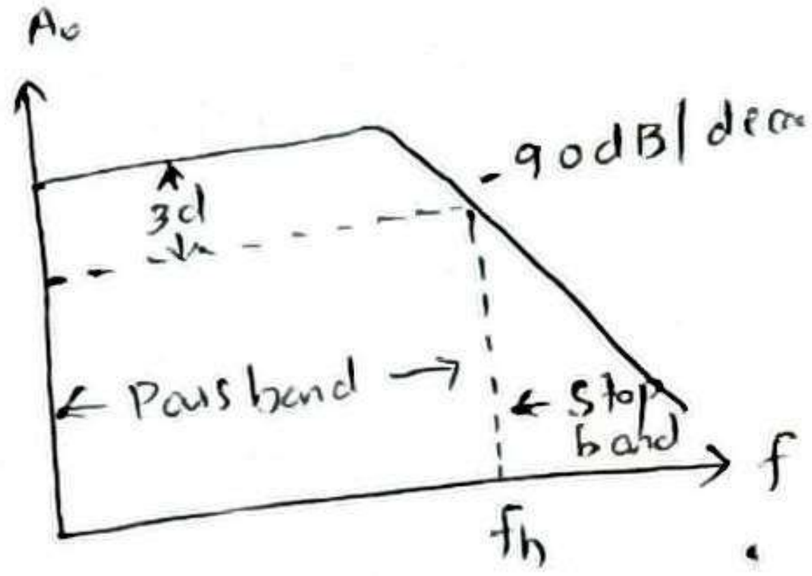
$$|H(j\omega)| = \frac{A_0}{\sqrt{1+\left(\frac{\omega}{\omega_h}\right)^4}} \rightarrow (13)$$

For 2nd order eqn (13) can be expressed as

$$\boxed{|H(j\omega)| = \frac{A_0}{\sqrt{1+\left(\frac{\omega}{\omega_h}\right)^{2\times 2}}}} \rightarrow (14)$$

For n^{th} order, it is expressed as

$$\boxed{|H(j\omega) = \frac{A_0}{\sqrt{1+\left(\frac{\omega}{\omega_h}\right)^{2n}}}} \rightarrow (15)$$



(x) (x) Design procedure for 2nd orde Butterworth LPF (for problems

① Choose a value of higher cut of freq 'fh'

② Let $R_2 = R_3 = R$ & $C_2 = C_3 = C$

→ Choose any value of $C \leq 1\mu f$

→ Then find 'R' value using

$$f_h = \frac{1}{2\pi\sqrt{R_2R_3C_2C_3}} = \frac{1}{2\pi RC}$$

$$\Rightarrow R = \frac{1}{2\pi f_h C}$$

③. Calculate pass band gain required to achieve BW response

$$A_0 = 3 - \alpha$$

$$\alpha = (1.414)$$

$$\Rightarrow A_0 = 3 - 1.414 = 1.586$$

WKT, gain $A_0 = 1 + \frac{R_f}{R_1}$ $\Rightarrow$

$$1 + \frac{R_f}{R_1} = 1.586$$

$$\frac{R_f}{R_1} = 0.586 \quad \therefore \boxed{R_f = 0.586 R_1}$$

(4) Choose value of $R_1 \leq 100\ k\Omega$

Find R_f using above eqn in 4th step

Select $R_L = 10k\Omega$

(5) Calculate gain magnitude (or) freq response from $\left(\frac{V_o}{V_{in}}\right)$

(2) High Pass Active Filter:

- High pass is compliment of LPF
- It is obtained by exchanging R and C in LPF ckt

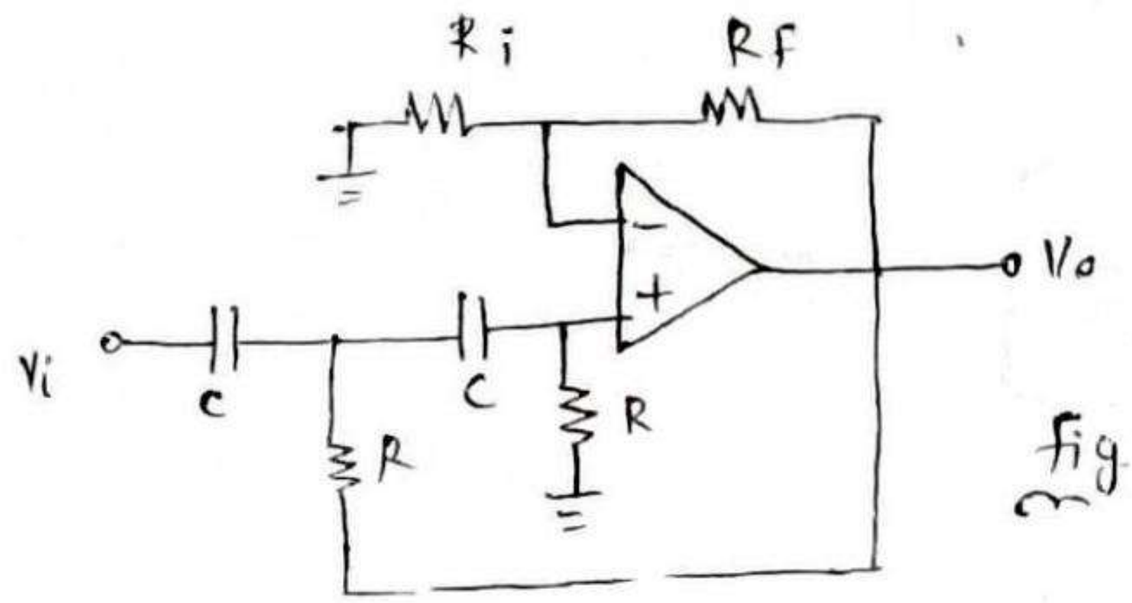


fig 2nd order HPF

Put $Y_1 = Y_2 = SC$; $Y_3 = Y_4 = \frac{1}{R}$ in eqn (7)

$$H(S) = \frac{A_0 (SC)(SC)}{(SC)^2 + (SC)\left(\frac{1}{R}\right)(1-A_0) + \frac{1}{R}\left(SC + SC + \frac{1}{R}\right)} \rightarrow (17)$$

After further simplification, the transfer function is

$$H(S) = \frac{A_0 S^2}{S^2 + (3 - A_0)\omega_J S + \omega_J^2} \rightarrow (18)$$

where, $\omega_J = 1/RC$

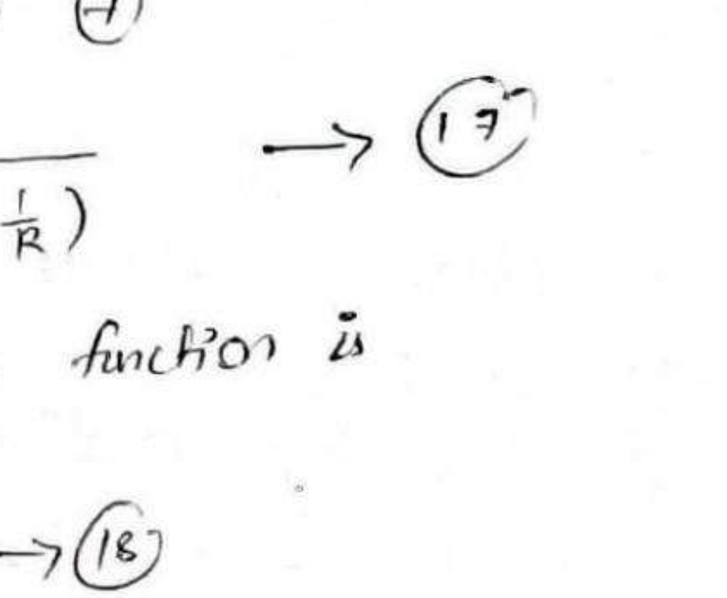
$$(\text{or}) \quad H(S) = \frac{A_0}{1 + \frac{\omega_J}{S}(3 - A_0) + \left(\frac{\omega_J}{S}\right)^2} \rightarrow (19)$$

For $\omega = 0 \Rightarrow H(S) = 0$

$\omega = \infty \Rightarrow H(S) = A_0$

The lower cut-off frequency is

$$f_J = f_{3dB} = \frac{1}{2\pi RC}$$



f_J - lower cut-off freq.

Putting $s = j\omega$ in (19) and 3 $A_0 - x = 1.414$

the voltage gain magnitude eqn of II order HPF is

$$|H(j\omega)| = \left|\frac{V_o}{V_i}\right| = \frac{A_o}{\sqrt{1+(f_1/f)^4}} \quad \rightarrow (20)$$

Hence, $$\left|\frac{H(j\omega)}{A_o}\right| = \frac{1}{\sqrt{1+\left(\frac{f_1}{f}\right)^4}} \quad \rightarrow (21)$$

For 2nd order HPF, the expression can be written as

$$\boxed{\left|\frac{H(j\omega)}{A_o}\right| = \frac{1}{\sqrt{1+(f_1/f)^{2\times 2}}}} \quad \rightarrow (22)$$

For n^{th} order HPF, it is

$$\boxed{\left|\frac{H(j\omega)}{A_o}\right| = \frac{1}{\sqrt{1+(f_1/f)^{2n}}}} \quad \rightarrow (23)$$

(3) Band pass filter:

There are 2 types of BPF as per quality factor Q

(a) Narrow band pass filter $(Q > 10)$

(b) Wide " $(Q < 10)$

The following relationship is important

$$Q = f_0 / BW = f_0/(f_h - f_1)$$

where $f_0 = \sqrt{f_h f_1}$

$f_0 \rightarrow$ central freq

$f_h \rightarrow$ upper cut-off freq

$f_1 \rightarrow$ lower cut-off freq

(a) Narrow Band Pass filter

Important parameters of BPF are

→ upper & lower cut off freq (f_h & f_1)

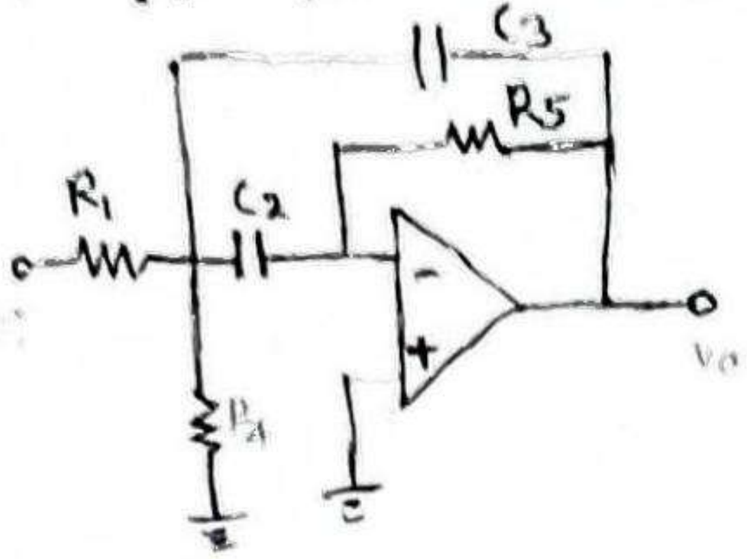
→ Band width (BW)

→ central freq (f_0)

→ Central freq. gain (A_0)

→ Selectivity (Q)

• ckt has 2 feedback path & Op-amp is in inverting mode



fig(a) 2nd order BPF

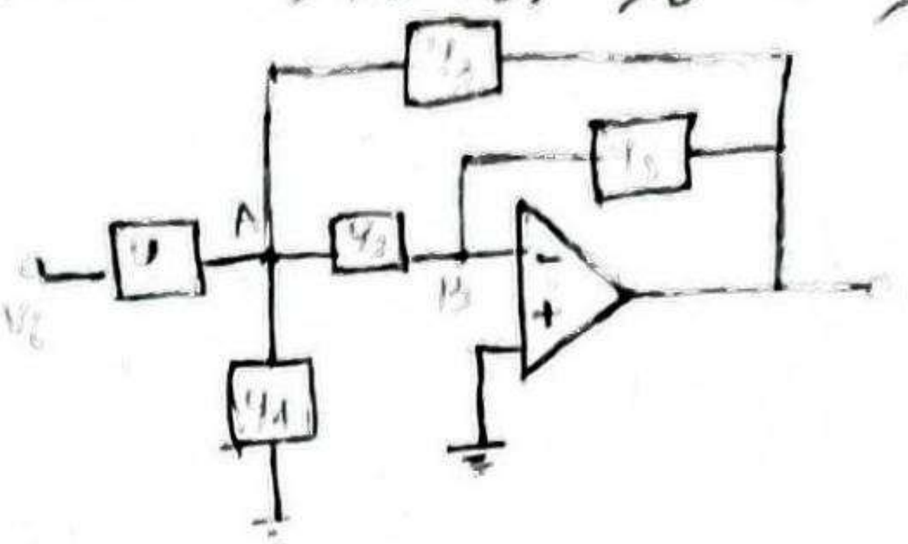


fig (b) Band-pass configuration.

Apply KCL at node 'A' in fig(a)

$$(V_A - V_i)Y_1 + (V_A - V_B)Y_2 + (V_A - V_o)Y_3 + V_A Y_4 = 0$$

$$Y_1 V_A - V_i Y_1 + V_A Y_2 - V_B Y_2 + V_A Y_3 - V_o Y_3 + V_A Y_4 = 0$$

$$V_A[Y_1 + Y_2 + Y_3 + Y_4] + V_i Y_1 - V_o Y_3 = 0 \quad (\because V_B = 0, \text{ the term } V_B Y_2 = 0)$$

$$\therefore V_i Y_1 + V_o Y_3 = V_A(Y_1 + Y_2 + Y_3 + Y_4) \longrightarrow (24)$$

KCL at node 'B'

$$(V_B - V_A)Y_2 + (V_B - V_o)Y_5 = 0$$

$$-V_A Y_2 - V_o Y_5 = 0 \quad (\because V_B = 0)$$

$$\Rightarrow V_A Y_2 = -V_o Y_5$$

$$\therefore \boxed{V_A = -V_o \frac{Y_5}{Y_2}} \longrightarrow (25)$$

Sub (25) in (24)

$$V_i Y_1 + V_o Y_3 = \frac{-V_o Y_5 (Y_1 + Y_2 + Y_3 + Y_4)}{Y_2}$$

$$V_i Y_1 = \frac{-V_o[Y_1 Y_5 + Y_2 Y_5 + Y_3 Y_5 + Y_4 Y_5)}{Y_2} - V_o Y_3$$

$$V_i Y_1 = \frac{-V_o(Y_1 Y_5 + Y_2 Y_5 + Y_3 Y_5 + Y_4 Y_5) - V_o Y_3 Y_2}{Y_2}$$

$$V_i Y_1 = \frac{+V_o[Y_1 Y_5 + Y_2 Y_5 + Y_3 Y_5 + Y_4 Y_5 + Y_2 Y_3)}{Y_2}$$

$$\Rightarrow \frac{V_o}{V_i} = \frac{-Y_1 Y_2}{Y_1 Y_5 + Y_2 Y_5 + Y_3 Y_5 + Y_4 Y_5 + Y_2 Y_3} \longrightarrow (26)$$

For this ckt to be BPF put $V_1 = G_4 V_0 = sC_3$, $V_3 = sC_3$, $V_0 = G_4$, $V_4 = G_5$

The Transfer fn becomes

$$H(s) = \frac{V_0(s)}{V_i(s)} = \frac{sG_1C_1}{G_1G_3 + sC_3G_5 + sG_3G_4 + G_4G_5 + s^2C_1C_3}$$

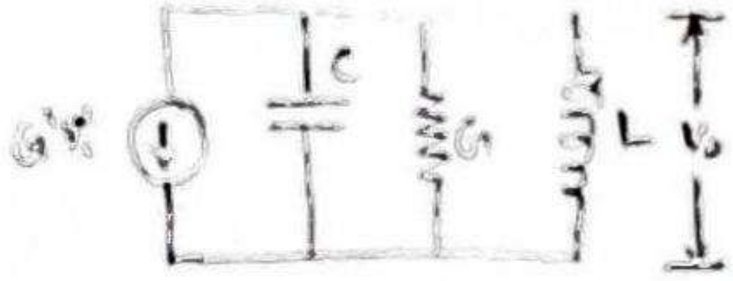
$$= \frac{sG_1C_3}{s^2C_1C_3 + s(G_3+G_4)C_3 + G_5(G_1+G_4)}$$

$$= \frac{-G_1}{sC_3 + s(G_3+G_4) + G_5(G_1+G_4)/C_3 s}$$

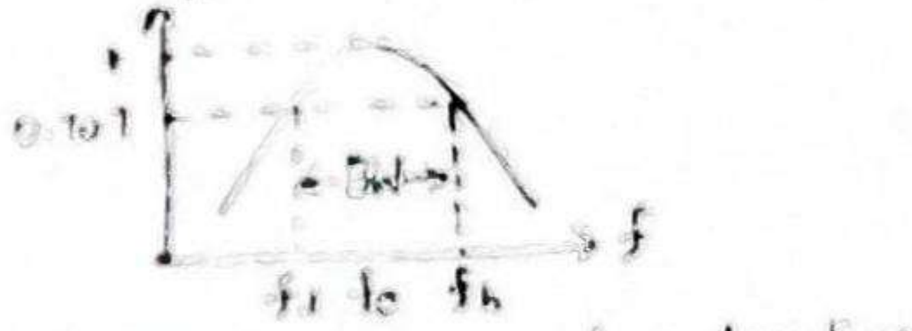
$$H(s) = \frac{-G_1}{sC_3 + \frac{G_5(G_1+G_4)}{C_3} + \frac{G_5(G_1+G_4)}{C_3 s}} \rightarrow (27)$$

The ckt is gain equivalent of a parallel RLC ckt of fig(c) driven by current source $G'V_i$ and with Bandpass characteristics as in fig(d)

The gain expression, $\frac{V_0(s)}{V_i'(s)} = \frac{-G'}{Y} = \frac{-G'}{sC + G_1 + 1/sL} \rightarrow (28)$



fig(c) Parallel RLC ckt



fig(d) Band-pass characteristics

Comparing gain expression in (27) & (28)

$$G' = G_1 \quad - (29)$$

$$L = \frac{C_2}{G_5(G_1+G_4)} \quad - (30)$$

$$G_1 = \frac{G_5(C_2+C_3)}{C_2} \quad - (31)$$

$$\& \quad C = C_3 \quad - (32)$$

At resonance the ckt fig(c) has unity power factor i.e imaginary part is zero which gives resonant freq ω_0 as

$$\omega_0^2 = \frac{1}{LC} = G_5\frac{(G_1+G_4)}{C_2C_3} \quad - (33)$$

(b) Wide BPF

Formed by cascading HPF & LPF section with Roll-off rate

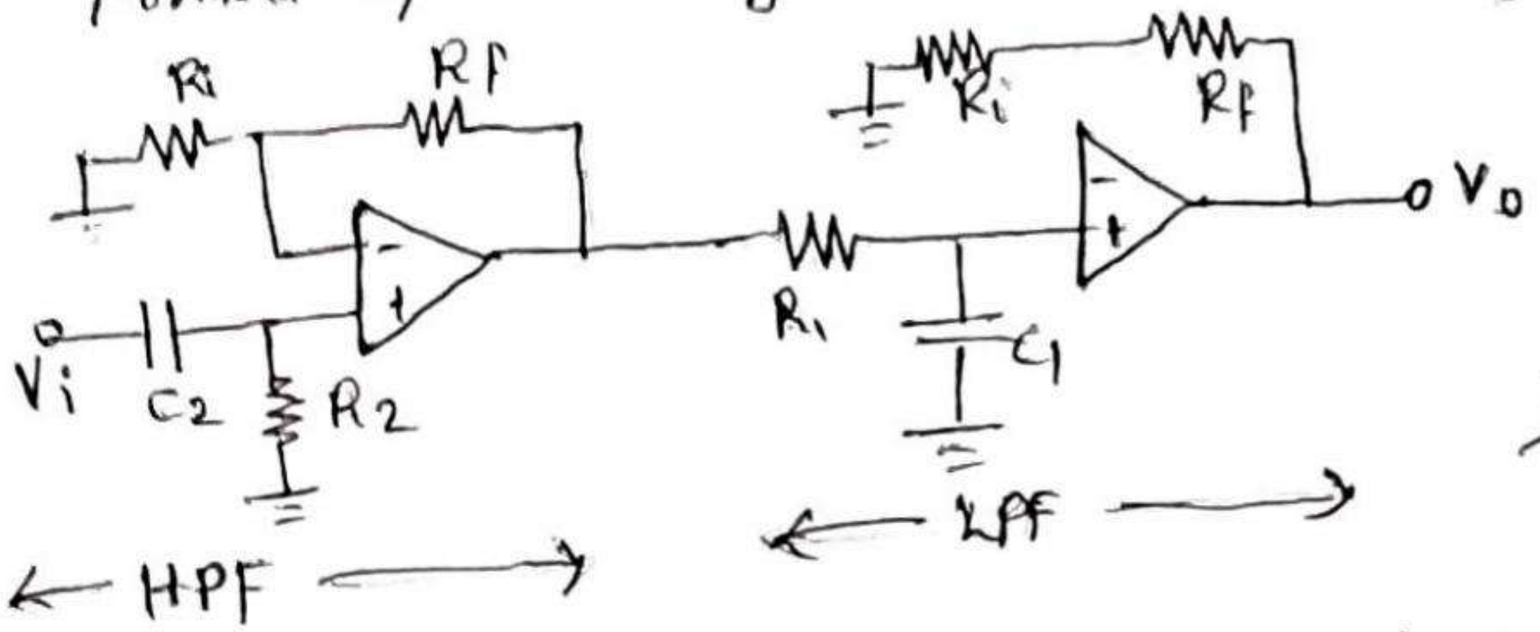


fig 1st order BPF

ist high pass section the magnitude of gain is

$$|H_{HP}| = \left|\left(1+\frac{Rf}{Ri}\right)\left(\frac{j2\pi f R_2 C_2}{1+j2\pi f R_2 C_2}\right)\right| = \left|A_{O1}\frac{j(f/fJ)}{1+j(f/fJ)}\right| = \frac{A_O(f/fJ)}{\sqrt{1+(f/fJ)^2}}$$

where, $f_J = \frac{1}{2\pi R_2 C_2}$

Similarly for low pass section,

$$|H_{LP}| = \frac{A_{O2}}{\sqrt{1+(f/fn)^2}}$$

where, $f_h = \frac{1}{2\pi R_1 C_1}$

The voltage gain magnitude of BPF is product of HPF & LPF

The freq response can be calculated from

$$\left|\frac{V_o}{V_i}\right| = \frac{A_O(f/fJ)}{\sqrt{[1+(f/fJ)^2][1+(f/f_h)^2]}}$$

where total pass band gain $A_O = A_{O1} \times A_{O2}$

To obtain -40 dB/decade roll-off, II order LPF & HPF should be cascaded

The gain at response is

$$\left.\frac{V_o}{V_i}\right|_{\omega=\omega_0} = -\frac{G_1}{G_4} - \frac{G_1}{G_4} = -\frac{(G_1 | G_5)C_2}{C_2+C_3}$$

$$= -\frac{(R_5/R_1)C_2}{C_2+C_3}$$

The Q-factor is

$$Q_0 = \frac{\omega_0 L}{R} = \omega_0 RC = \frac{\omega_0 C}{G_4} = \frac{\omega_0 C_2 C_3}{(C_2+C_3)G_5} \quad -(36)$$

The bandwidth is given by

$$BW = f_h - f_l = \frac{f_0}{Q_0} = \frac{\omega_0}{2\pi Q_0} = \frac{\omega_0}{2\pi R C_2 C_3}$$

$$= \frac{1}{2\pi RC} = \frac{G_4}{2\pi C} = \frac{G_5(C_2+C_3)}{2\pi C_2 C_3}$$

and $f_0 = \sqrt{f_h f_l}$

For $C_2 = C_3 = C$, the gain from eqn (32) is

$$\left.\frac{V_o}{V_i}\right|_{\omega=\omega_0} = -\frac{R_5}{2R_1} = -A_0 \quad \rightarrow (37)$$

$$\omega_0 = \frac{\sqrt{G_5(G_1+G_4)}}{C} \quad \rightarrow (38)$$

$$BW = \frac{G_5}{\pi C} = \frac{1}{\pi R_5 C} \quad \rightarrow (39)$$

Above (3) eqn are gain at resonance, resonance freq. & bandwidth

Using eqn (35), (37) & (38) in eqn (27), transfer fn becomes:

$$H(S) = \frac{-A_0(\omega_0/Q)S}{S^2 + (\omega_0/Q)S + \omega_0^2} \quad \rightarrow (40)$$

$$= \frac{-A_0 \alpha \omega_0 S}{S^2 + \alpha\omega_0 S + \omega_0^2} \quad \rightarrow (41)$$

For $\omega \ll \omega_0$ and $\omega \gg \omega_0 \Rightarrow$ gain $= 0$

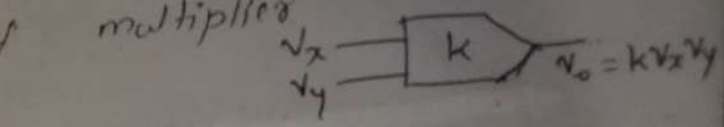
$\omega = \omega_0$, gain $= A_0$

Analog multipliers: [Analog Multipliers]

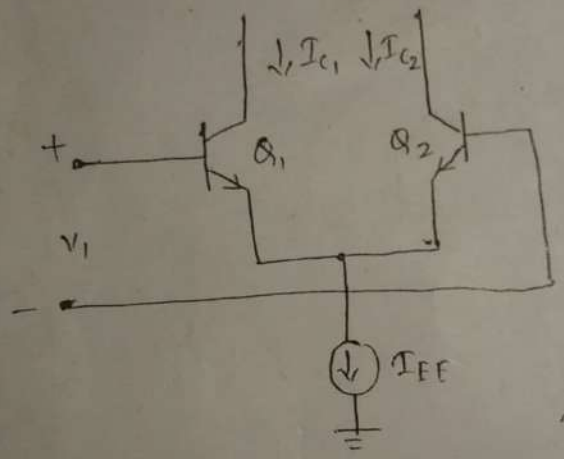
- It is most commonly used technique & integrated ckt component for performing non-linear operations on signals. Gilbert multiplier cell forms basis of a wide variety of ckt $[V_o = K V_x V_y]$

Common terminologies associated with multiplier characters:

1. Accuracy : deviation of actual o/p from ideal o/p
2. Linearity : defines accuracy of multiplier
3. Squaring mode accuracy
4. Bandwidth



1.11 Analog Multiplier using Emitter Coupled Transistor pair



$$I_B = I_C \left[1 + e^{-V_B/V_T}\right]$$

fig. Emitter coupled transistor pair

The o/p currents I_{C1} and I_{C2} are related to V_1 is given

$$I_{C1} = \frac{I_{EE}}{1 + e^{-V_1/V_T}} \longrightarrow (1)$$

$$I_{C2} = \frac{I_{EE}}{1 + e^{V_1/V_T}} \longrightarrow (2)$$

where V_T is thermal voltage.

I_{B1} & I_{B2} are neglected

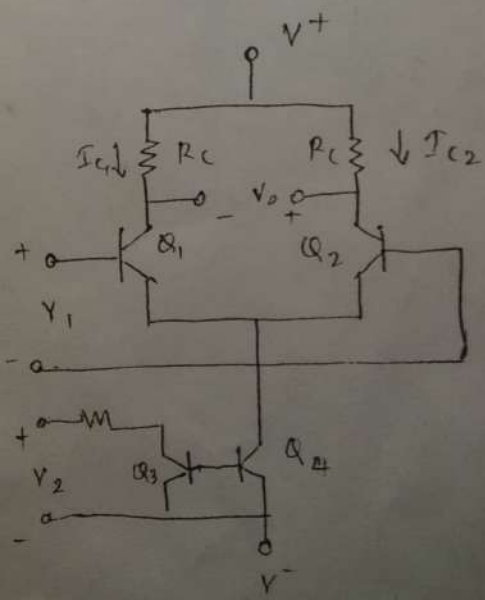


fig (b) Simple modulator using differential amp

From ① & ②

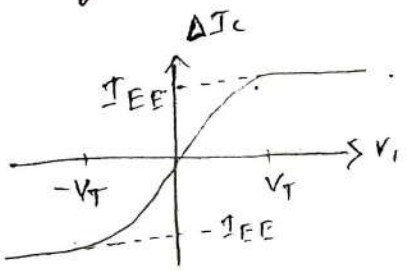
$$\Delta I_C = I_{C1} - I_{C2}$$

$$= \frac{I_{EE}}{1+e^{-V_1/V_T}} - \frac{I_{EE}}{1+e^{V_1/V_T}}$$

$$= I_{EE}\left[\frac{1}{1+e^{-V_1/V_T}} - \frac{1}{1+e^{V_1/V_T}}\right]$$

$$\therefore \Delta I_C = I_{EE} \tanh\left(\frac{V_1}{2V_T}\right) \rightarrow ③$$

The dc transfer characteristics of Emitter-coupled transistor pair is given



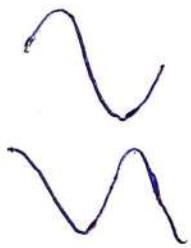
When $V_1 << V_T$, $I_{EE}\tanh\left(\frac{V_1}{2V_T}\right) = I_{EE}\frac{V_1}{2V_T}$ → ④

Thus eqn ③ becomes, $\Delta I_C = I_{EE}\left(V_1/2V_T\right)$ → ⑤

→ If I_{EE} is proportional to 2nd i/p signal V_2 then

$$I_{EE} \simeq k_0[V_2 - V_{BE(on)}] \rightarrow ⑥$$

Sub ⑥ in ⑤, $\Delta I_C = \frac{k_0 V_1 [V_2 - V_{BE(on)}]}{2V_T} \rightarrow ⑦$



There are 2 limitations in this.

① V_2 is offset by $V_{BE(on)}$ ② V_2 must always be positive.

③ $\tanh(x)$ is approximated as 'x'.

To over come 1st 2 limitation Gilbert multiplier cell is used

12. Gilbert Multiplier cell

- It is modification of emitter coupled transistor cell and it allow four quadrant multiplication
- It is basis of integrated ckt balanced multipliers
- Two cross-coupled emitter-coupled pairs are in series connection with an emitter coupled pair forms Gilbert multiplier cell

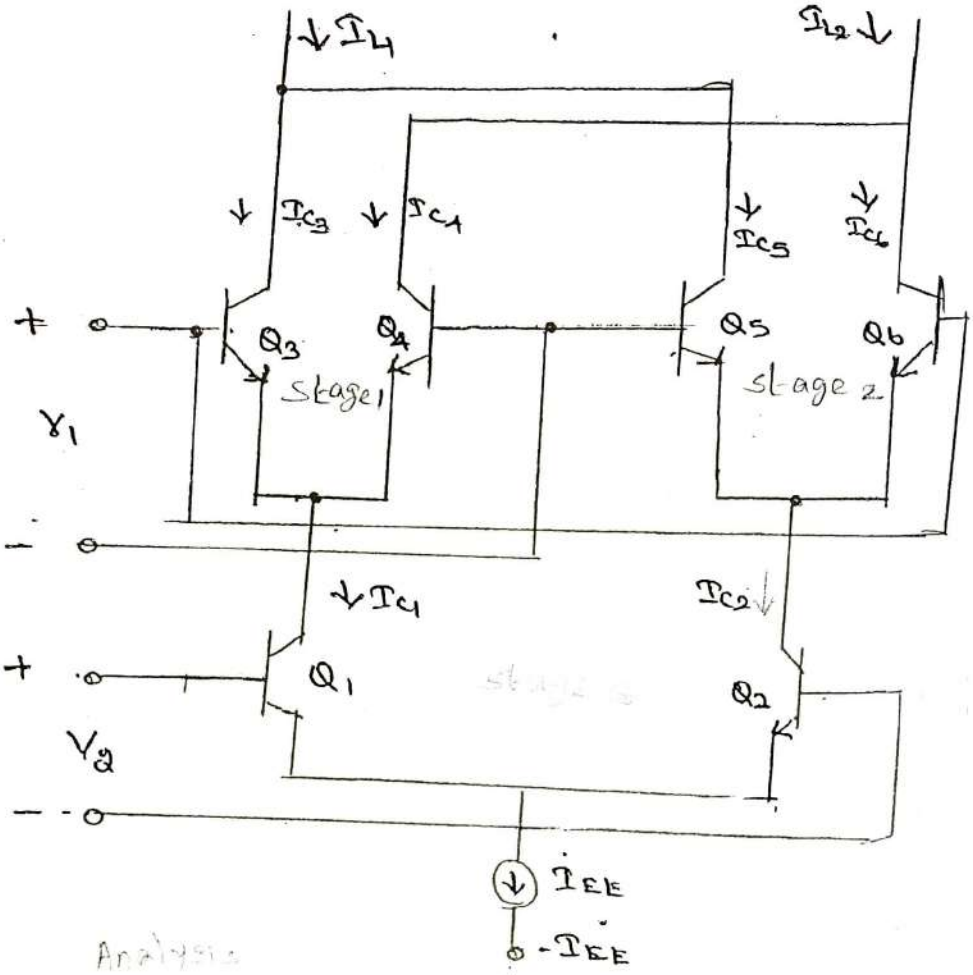
Collector currents of Q_3 & Q_4 are

$$I_{C3} = \frac{I_{C1}}{1+e^{-V_1/V_T}} \rightarrow ① \qquad I_{C4} = \frac{I_{C1}}{1+e^{V_1/V_T}} \rightarrow ②$$

The collector current of Q5 & Q6 are given by

$$I_{C5} = I_{C2} / 1 + e^{V_1/V_T} \rightarrow (3)$$

$$I_{C6} = \frac{I_{C2}}{1 + e^{-V_1/V_T}} \quad - (4)$$



Gilbert Multiplier cell

The collector currents I_{C1} & I_{C2} of transistor Q_1 & Q_2 can be expressed as

$$I_{C1} = \frac{I_{EE}}{1 + e^{-V_2/V_T}} \quad - (5)$$

$$I_{C2} = \frac{I_{EE}}{1 + e^{V_2/V_T}} \quad - (6)$$

Sub (5) in (1) & (2)

$$I_{C3} = \frac{I_{EE}}{(1 + e^{-V_1/V_T})(1 + e^{-V_2/V_T})} \quad - (7)$$

$$I_{C4} = \frac{I_{EE}}{(1 + e^{V_1/V_T})(1 + e^{-V_2/V_T})} \quad - (8)$$

Substitute (6) in (3) & (4)

$$I_{C5} = \frac{I_{EE}}{(1+e^{V_1/V_T})(1+e^{V_2/V_T})} \quad - (9)$$

$$I_{C6} = \frac{I_{EE}}{(1+e^{-V_1/V_T})(1+e^{V_2/V_T})} \quad - (10)$$

The differential o/p current ΔI is given by.

$$\Delta I = I_{L1} - I_{L2}$$

$$\Delta I = (I_{C3} + I_{C5}) - (I_{C4} + I_{C6})$$

$$\Delta I = (I_{C3} - I_{C6}) - (I_{C4} - I_{C5}) \quad - (11)$$

Substitute eq (1) in (10) in (11) & employing expriential formulae for hyperbolic functions we get.

$$\Delta I = I_{EE}\left[\tanh\left(\frac{V_1}{2V_T}\right)\tanh\left(\frac{V_2}{2V_T}\right)\right] \quad - (12)$$

The above equation shows that when V_1 & V_2 are small, Gilbert cell shown in figure can be used as a four quadrant analog multiplier cell with use of current to voltage converters.

The dc transfer characteristics of such a multiplier circuit is the product of hyperbolic tangent of 2 i/p voltages. The o/p voltage V_o can be generated from ΔI, by using 2 equal valued resistors connected to V_{CC} & by sending I_{L1} ($= I_{C3} + I_{C5}$) thro' one resistor & I_{L2} ($= I_{C4} + I_{C6}$) thro' another (2) resistor.

A modulator or a mixer is a circuit with 2 i/p namely carrier i/p & modulating i/p & one modulated o/p. ①

Linear response is required only for modulating i/p, since carrier is usually an ac signal.

Multiplier can also be used as modulator., if one of the i/p's is very large & and i/p is very small ($\tanh(x) \approx x$)

Then, transistor operated by large signal i/p act as switches multiplies small i/p signal by square wave.

Hence this mode of operation act as modulator. = Synchronous Modulator.

[Gilbert multiplier with predistortion circuits]

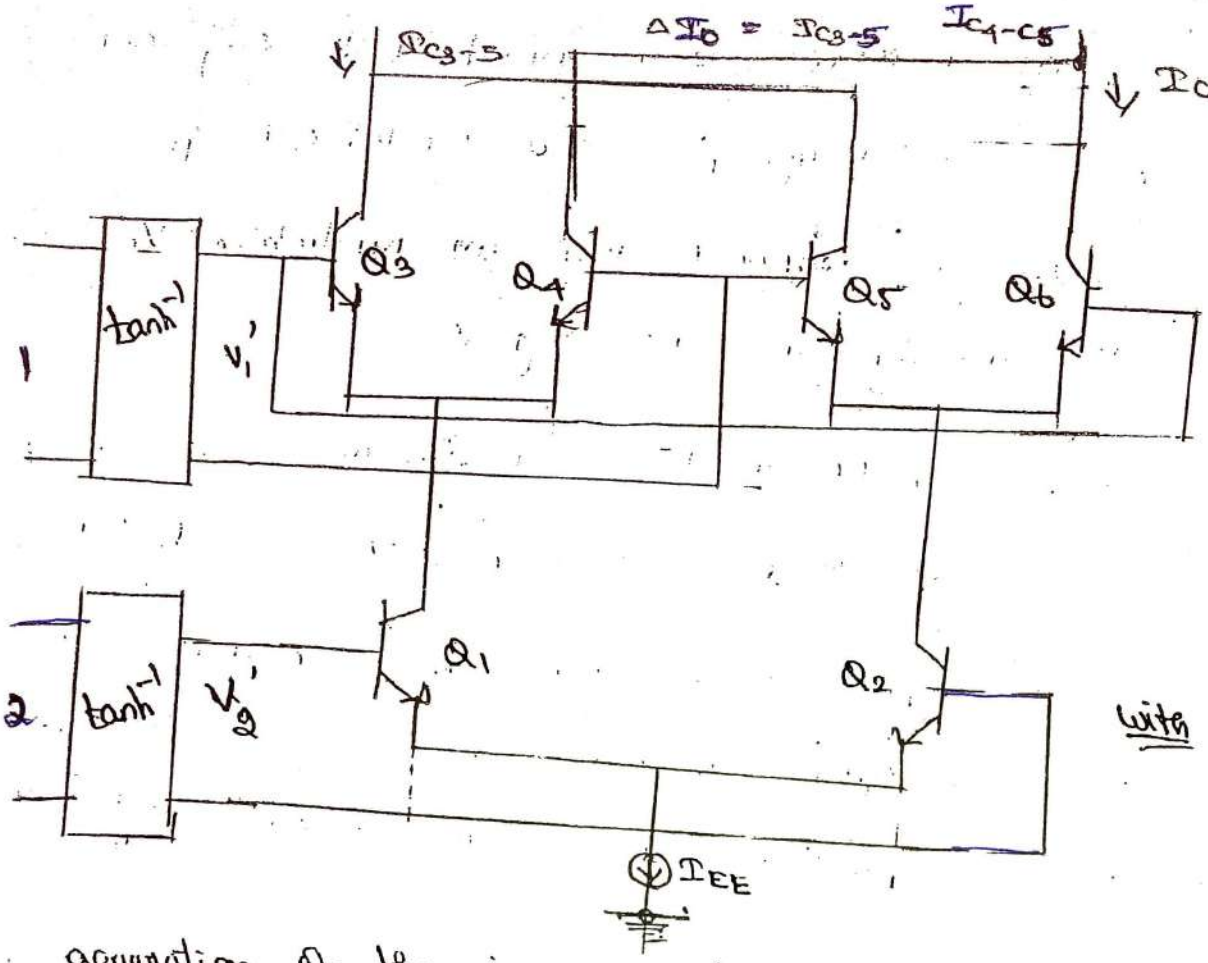
Gilbert Multiplier with Predistortion Circuits:

* when magnitude of V_1 & V_2 are very small when impared with V_T, the hyperbolic tan function is approximated as near, & circuit can be used as multiplier, for finding $V_1 \times V_2$.

But when larger V_1 & V_2 are to be multiplied, a non-linearity function can be used to predistort the i/p signal.

iis compensates for the hyperbolic tangent function transfer characteristics of basic cell.

Required non-linearity function is an "inverse hyperbolic tangent" characteristics.



Gilbert Multiplier circuit with Predistortion.

: generation of the inverse hyperbolic tangent function is shown above figure.

Assume that the circuit within the box generate a differential o/p current, & it linearly depends on i/p voltage V_1

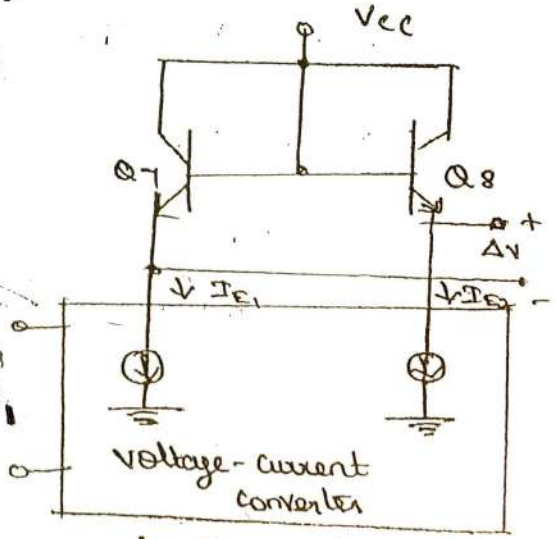
Then, $I_{E1} = I_{O1} + K_1 V_1$

$I_{E2} = I_{O1} - K_1 V_1$

I_{O1} = dc current flowing in each o/p.

K_1 = transconductance of voltage to current converter.

assume $V_1 = 0$.



An Inverse hyperbolic tangent circuit

The differential voltage ΔV across diode connected transistor Q_7 & Q_8 is given by

$$\Delta V = V_t \ln\left(\frac{I_{O1} + K_1 V_1}{I_O}\right) - V_T \ln\left(\frac{I_{O1} - K_1 V_1}{I_O}\right)$$

$$\Delta V = V_T \ln\left(\frac{I_{01} + K_1 V_1}{I_{01} - K_1 V_1}\right)$$

This can be transformed into

$$\Delta V = 2V_T \tanh^{-1}\left(\frac{K_1 V_1}{I_{01}}\right)$$

using identity $\tanh^{-1} = \frac{1}{2}\ln\left(\frac{1+x}{1-x}\right)$

is functional block is used, it compensates for the in- linearity of the i/p's

Eq: (12) can be represented by

$$\Delta I \simeq I_{EE}\left(\frac{K_1 V_1}{I_{01}}\right)\left(\frac{K_2 V_2}{I_{02}}\right) \quad - (13)$$

I_{01}, K_1, K_2 = parameters of the functional blocks following i/p V_1 & V_2.

complete Four - Quadrant Analog Multiplier:

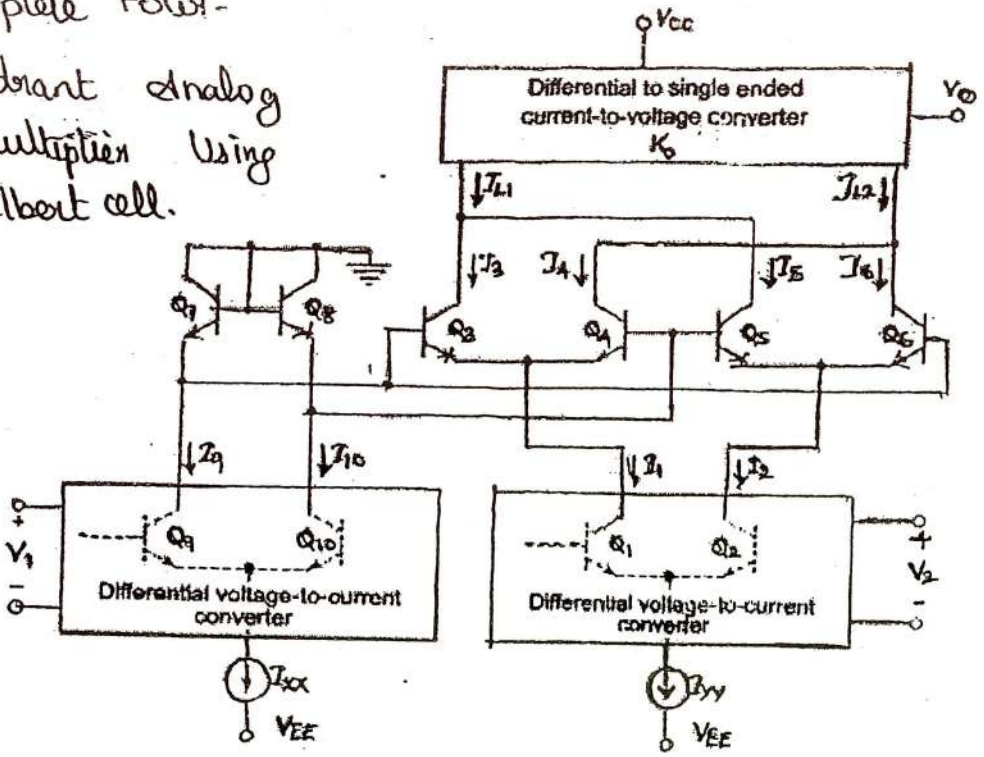
[Complete Four - Quadrant Analog Multiplier]

* The three boxes are voltage -to current converters or vice versa to voltage converters in effect.
* The pre- distortion for the input signal is achieved by transistor Q_1 & Q_8.
* The current I_q & I_{bo} passing through the emitter of Q_7 & generate a voltage between the two emitter terminals, that is proportional to the inverse hyperbolic tangent of V_1
* This compensates for the hyperbolic tangent expression for eq. (8), I_{C4}.

lysis of the circuit:

A complete four quadrant analog multiplier using Gilbert cell is shown in below figure.

1 Complete Four-Quadrant Analog Multiplier Using - Gilbert cell.



2 current through base-emitter junctions of transistors Q_{10}, Q_3, Q_4, & Q_9 connected in series can be expressed by.

$$I_9 I_3 = I_4 I_{10} \quad -(14)$$

III/y from the series connection of the transistor Q_7, Q_6, Q_5 and Q_8, we get.

$$I_9 I_6 = I_5 I_{10} \quad -(15)$$

From (11), we get

$$I_1 = I_3 + I_4 \quad -(16)$$

$$I_2 = I_5 + I_6 \quad -(17)$$

$$I_{L1} = I_3 + I_5 \quad -(18)$$

$$I_{L2} = I_4 + I_6 \quad -(19)$$

$$I_{XX} = I_9 + I_{10} \quad -(20)$$

The transfer characteristics of differential voltage to current converter is given by

$$I_9 - I_{10} = \frac{V_1}{K_1} \quad -(21) \quad \& \quad I_1 - I_2 = \frac{V_2}{K_2} \quad -(22)$$

1 the transfer characteristics of the differential-to-single fed current to voltage converter is given by

$$V_o = K_o (I_{L2} - I_4) \quad - (23)$$

Where K_o, K_1, K_2 = constants.

Substitute for I_4 & I_{L2} from (18) & (19) in (23)

$$V_o = K_o [(I_4 + I_6) - (I_3 + I_5)]$$

Using eq (14) & (15),

$$V_o = K_o \left[\left(I_4 + I_5 \frac{I_{10}}{I_9} \right) - \left(I_4 \frac{I_{10}}{I_9} + I_5 \right) \right] - (24)$$

Simplifying the above eq.

$$V_o = K_o \left(\frac{I_9 - I_{10}}{I_9} \right) (I_4 - I_5) \quad - (25)$$

From (16) & (17)

$$I_1 - I_2 = (I_3 + I_4) - (I_5 + I_6)$$

$$= \left(I_4 \frac{I_{10}}{I_9} + I_4 \right) - \left(I_5 + I_5 \frac{I_{10}}{I_9} \right)$$

Solving for $(I_4 - I_5)$ gives ... (26)

$$(I_4 - I_5) = \left(\frac{I_9}{I_9 + I_{10}} \right) (I_1 - I_2) \quad - (27)$$

Sub (27) in (25) & using (21) & (22), we get

$$V_o = K_o \left(\frac{I_9 - I_{10}}{I_9 + I_{10}} \right) (I_1 - I_2)$$

$$= \frac{K_o V_1 V_2}{I_{xx} K_1 K_2} = K_m V_1 V_2 \quad - (28)$$

where $K_m = \dfrac{K_o}{I_{xx} K_1 K_2}$

(28) employs no approximations. Hence the i/p s/g amplitudes have no constraints.

Practical

Implementation of 4-Quadrant Analog Multiplier

It can be observed that

$$I_1 - I_2 = \frac{2 V_2}{R_4} \quad \rightarrow (29)$$

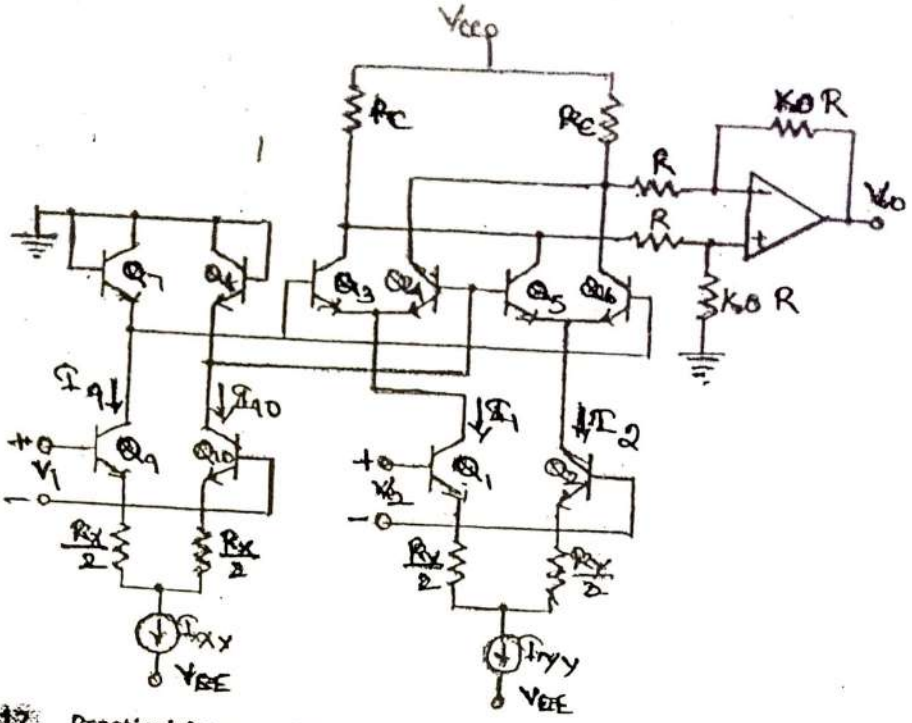


Fig. 9.12 Practical four-quadrant analog multiplier circuit

$$I_9 - I_{10} = \frac{2V_1}{R_x} \quad - (30)$$

further it is assumed that the drop across base-emitter of $Q_9 - Q_{10}$ & $Q_1 - Q_2$ pairs are small in comparison with the drop across R_x & R_y

Sub (29) & (30) in (28)

$$V_o = \frac{4 K_o R_c V_1 V_2}{I_{xx} R_x R_y}$$

$$= K_m V_1 V_2 \quad \text{where } R \gg R_c.$$

This circuit is capable of performing precise multiplication of continuously varying analog signal by another signal.

problem:

- Need to be able to trim the errors due to offset & Mismatch in the integrated circuit implementation.

Variable Transconductance Techniques:

Variable Transconductance Technique:

Variable transconductance technique makes use of the depedence characteristics of the transistor transconductance parameter on the emitter current bias applied.

Simple differential circuit arrangement depicting the principle is shown in below figure.

The relationship between V_O & V_x is given by

$$V_O = g_m R_L V_x \longrightarrow (30)$$

$g_m = I_{EE}/V_T$ = transconductance of the stage.

Application of 2nd i/p V_y to reefference current source of the differential amplifier in vary g_m.

Thus, if $R_E I_{EE} \gg V_{BE}$, the bias voltage is related to I_{EE} by the relation $V_y = I_{EE} R_E$.

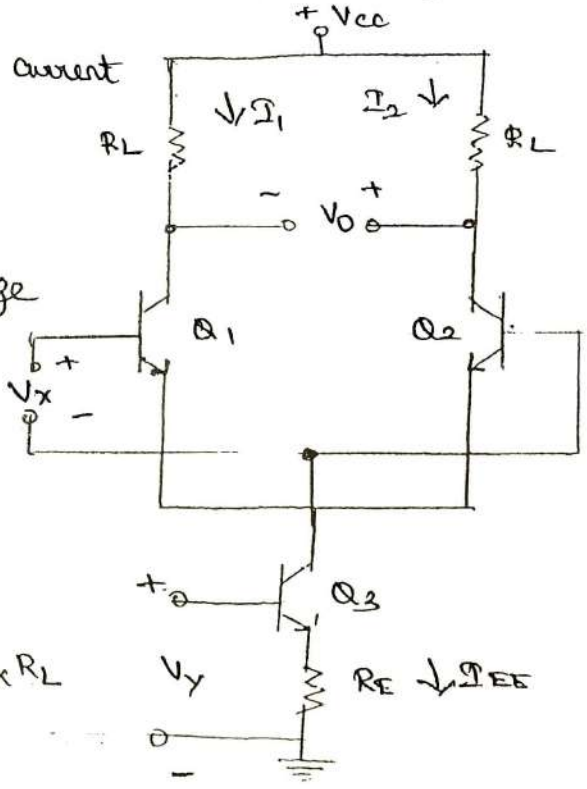


Fig: Differential stage of Transconductance Multiplier

Thus the overall voltage transfer Expression is given by

$$V_O = g_m R_L V_x = (V_y / V_T R_E) V_x R_L$$

$$= V_x V_y \frac{R_L}{V_T R_E}$$

Operation of Logarithmic Bias Input for Differential Stage:

It is assumed that $|V_x| << V_y$ ∴ there is no emitter generation.

Ref. Eq (4), collector current I_1 & I_2 are related to the applied voltage V_x by the relation

$$\frac{I_1}{I_2} = e^{(V_x/V_y)} \longrightarrow (31)$$

linearity can be achieved by reducing the exponential current-voltage characteristics to a linear one as shown in 38.

The transistor Q_1 & Q_2 are biased through the diode connected Q_A & Q_B, which are driven by controlled current source I_A & I_B respectively.

Then the net bias voltage V_x is represented by.

$$V_x = V_T \ln (I_B/I_A) \quad - (32)$$

Sub (32) in (31)

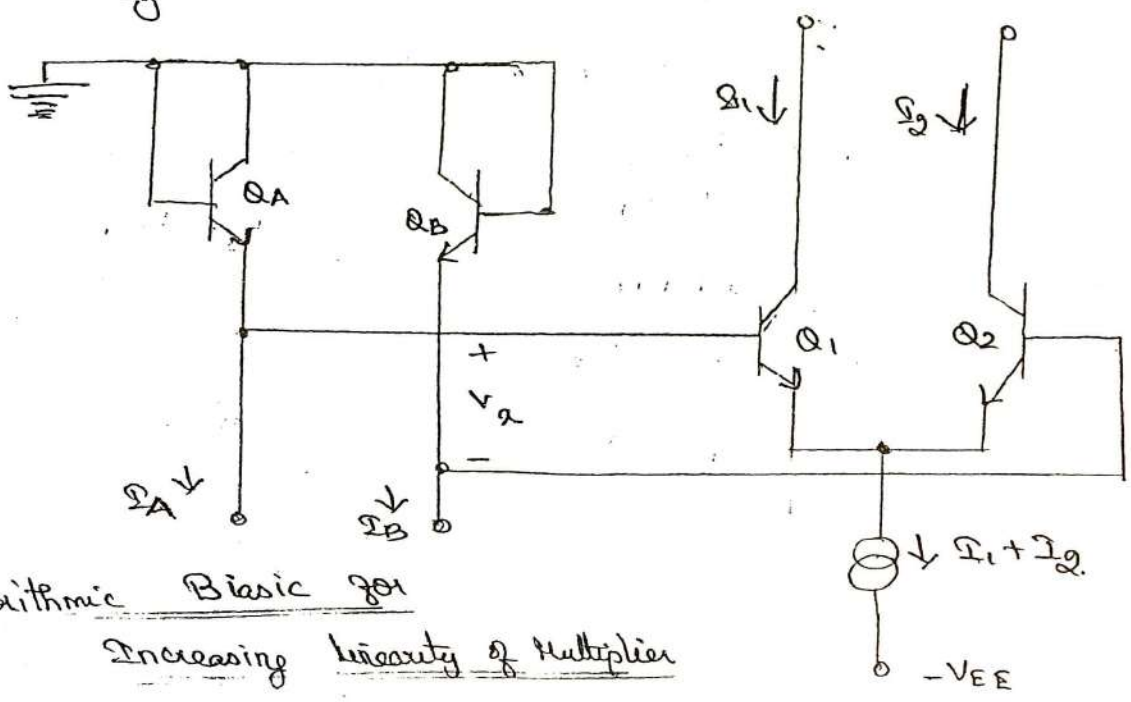
$$\frac{I_1}{I_2} = \frac{I_B}{I_A}$$

W.K.T

$$\frac{I_A}{I_A+I_B} = \frac{I_2}{I_1+I_2} = \frac{1}{1+e^{V_x/V_T}} \quad - (33)$$

$$\frac{I_B}{I_A+I_B} = \frac{I_1}{I_1+I_2} = \frac{e^{V_x/V_T}}{1+e^{V_x/V_T}} \quad - (34)$$

The above equation are valid over a wide range, of the device characteristics are well matched & V_{BE} obey basic diode equation.

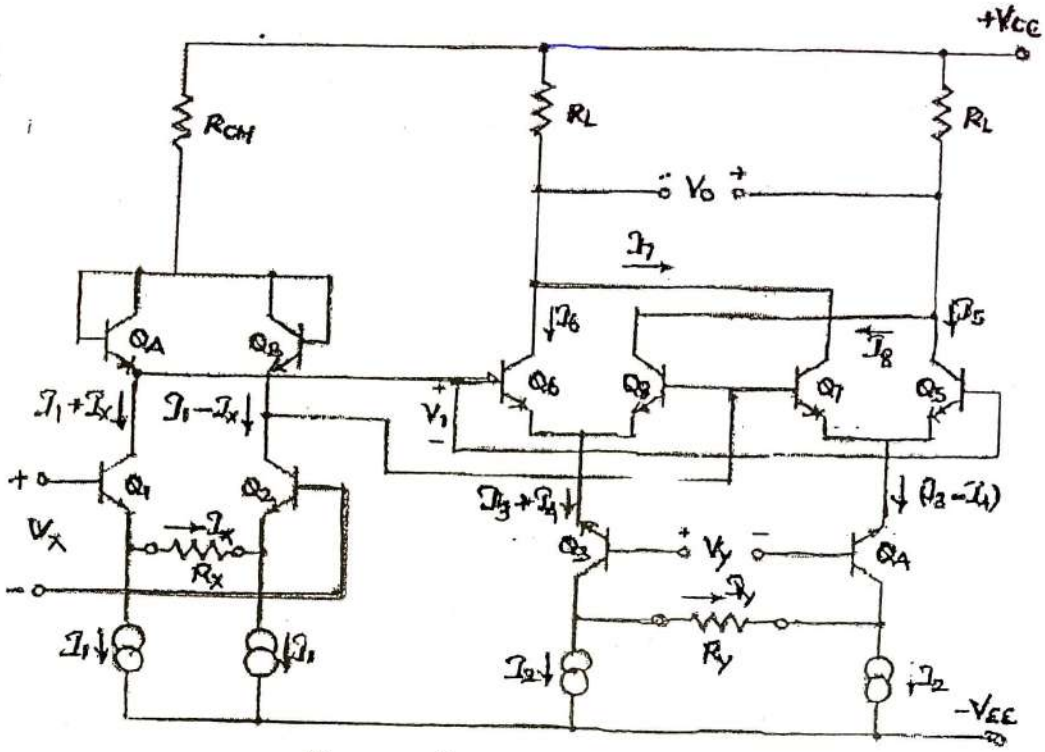


Logarithmic Biasic for Increasing linearity of Multiplier

Four Quadrant Variable Transconductance Multiplier:

Four Quadrant Variable Transconductance Multiplier.

A typical four-quadrant multiplier circuit is shown below.



FOUR. QUADRANT MONOLITHIC MULTIPLIER

The four quadrant operation indicates that the o/p voltage is directly proportional to the product of the 2 i/p voltage regardless of the polarity of the i/p's and such multipliers can be operated in all the four quadrants of operation.

The 1st part of circuit generates an intermediate voltage V_1 across the transistor Q_A & Q_B in response to i/p signal V_x.

The non-linear response to i/p V_x in generating V_1 is compensated by the inverse non-linearity associated with the base-emitter junctions of the quad-transistors. $Q_5 - Q_6$ & $Q_7 - Q_8$.

Thus the o/p voltage V_o is maintained proportional to the linear product of the 2 i/p voltages.

The emitter degeneration resistors R_x & R_y provide linear conversion of the i/p voltages to the differential currents I_x & I_y

Thus $I_x = \frac{V_x}{R_x}$ & $I_y = V_y/R_y$.

The value of R_x & R_y are chosen such that $R_x \gg V_T/I_1$ & $R_y \gg V_T/I_2$.

O/p voltage V_0 can be written as

$$V_0 = R_L ((I_6 + I_7) - (I_5 + I_8)) \quad - (35)$$

Apply (33) & (34) to the circuit,

$$\frac{I_6}{I_2+I_y} = \frac{I_5}{I_2-I_y} = \frac{I_1+I_x}{2I_1} \quad - (36)$$

& $$\frac{I_8}{I_2+I_y} = \frac{I_7}{I_2-I_y} = \frac{I_1-I_x}{2I_1} \quad - (37)$$

Sub (36) & (37) in (35).

$$V_0 = \frac{2R_L}{I_1}(I_x I_y) \quad - (38)$$

Since I_x & I_y are linearly related to V_x & V_y,

$$V_0 = K V_x V_y \quad - (39)$$

K = Scaling factor $= \frac{2R_L}{I_1 R_x R_y} = 0.1$.

APPLICATIONS OF MULTIPLIER Ic's

- → Voltage Squarer
- → Frequency Doubler
- → voltage divider
- → Square Rooter
- → Phase angle detector
- → Rectifier

Voltage Squarer :-

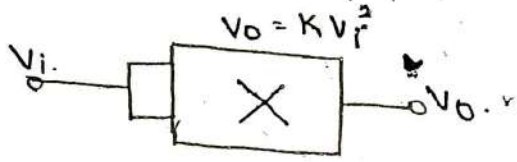


Fig shows Multiplier Ic connected as a squaring ckt. The i/p's can be positive or negative, represented by any corresponding voltage level between 0 & 10V.

I/p voltage V_i is squared simply by connecting both the terminal

$\therefore V_x = V_y = V_i$ & o/p is $V_o = KV_i^2$

The circuit thus perform the squaring operation. This application can be extended for frequency doubling applications also as explained.

Frequency Doubler :-

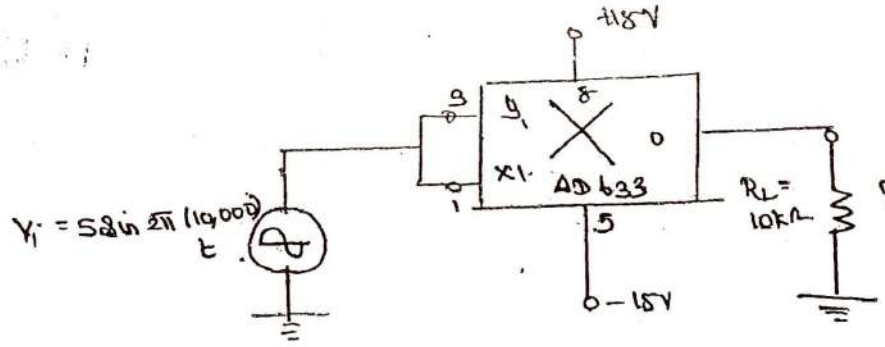
* Squaring circuit connected for frequency doubling operation.

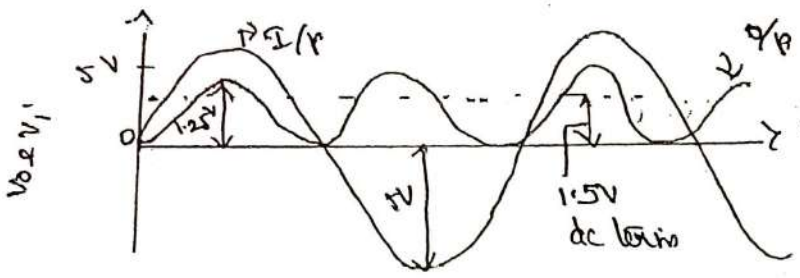
A sine wave signal V_i has a peak amplitude of A_V & frequency of f Hz

o/p voltage of doubler ckt is

$$V_o = \frac{A_V \sin 2\pi ft \times A_V \sin 2\pi ft}{10} = \frac{A_V^2}{10} \sin^2(2\pi ft)$$

$$= \frac{A_V^2}{20} [1 - \cos 4\pi ft]$$





fig(a) circuit diagram
fig(b) I/P & O/P waveform

Assume peak amplitude $A_V = 5V$ & $f = 10KHz$, $V_o = 1.25 - 1.25\cos 2\pi(2000)t$

1st term → dc term of 1.25 V peak amplitude

O/P waveform ripples with twice the i/p frequency in the rectified o/p of the i/p signal.

This forms principle of application of analog multiplier as rectifier of ac s/l

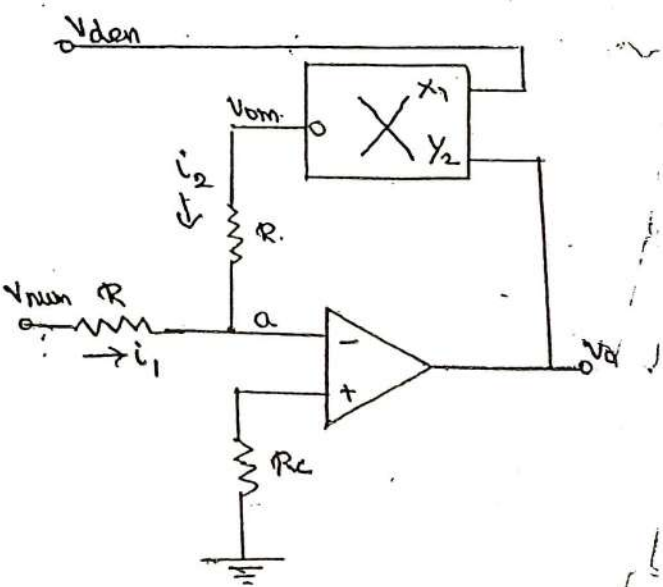
Dc component is removed by connecting 1μF coupling capacitor between o/p terminal & load resistor.

Voltage Divider:

Voltage divider constructed using multiplier & op-amp.

Circuit produces the ratio of 2 i/p s/l 's.

Division is achieved by connecting the multiplier in the feedback loop of an op-amp.



Two i/p voltages = V_{den} & V_{num}.

V_{den} = i/p of multiplier & o/p of op-amp V_{OA} as another i/p to multiplier.

O/p V_{om} of multiplier is connected back to inverting i/p of op-amp in feedback loop

Characteristic Eqn operation of multiplier gives $V_{om} = K V_{oA} V_{den}$

∴ shown in dia, NO i/p s/l current can flow into the inverting i/p terminal of op-amp. which is at virtual ground.

$V_{om} = K V_{oA} V_{den}$

∴ at 'a', $i_1 + i_2' = 0$

$i_1 = \frac{V_{num}}{R}$, R = i/p resistance

$i_2 = \frac{V_{om}}{R}$

With virtual Ground, at 'a'

$$i_1 + i_2 = \frac{V_{num}}{R} + \frac{V_{om}}{R} = 0$$

$$V_{om} = -V_{num}$$

Sub. V_{om} in above Eqn. $\Rightarrow K V_{oA} V_{den} = -V_{num}$

$$V_{oA} = \frac{-V_{num}}{K V_{den}}$$

where,

V_{num} & V_{den} are numerator & denominator voltages. ∴ voltage division operation is done.

V_{num} = '+'ve or '-' ve & V_{den} = only '+' ve value to ensure "-ve" feedback.

V_{den} is changed ; Gain $\propto 1/V_{den}$ changes, this feature is used in Automatic Gain control (AGC) circuits.

Square Rooter:-

Divider circuit can be used to find square root of a signal by connecting both i/p's of multiplier to o/p of op-amp.

o/p voltage of multiplier V_{om} is equal in magnitude but opposite in polarity (w.r.t Gnd) to V_i

W.K.T $V_{om} = (1/10)^{\text{Scale factor}} \text{ of } V_o \times V_o$ or.

$$-V_i = V_{om} = V_o^2/10$$

Solving for V_o & eliminating $V-1$ yields

$$V_o = \sqrt{10|V_i|}$$

* V_o = Square root of 10 times the absolute magnitude of V_i.
* V_i = must be negative or else op-amp saturates.
* Range of V_i is between -1 & $-10V$, voltage less than $-1V$ will cause inaccuracies.
* Diode prevents negative saturation for positive polarity V_i s/l.

For +ve value of V_i, diode connections are reversed.

Phase Angle Detector :-

Multiplier is configured as phase angle detection measurement. When 2 sine-waves of the same frequency are applied to the i/p of the multiplier, o/p V_o has a dc component & an ac component

Trignometric identity

$$\sin A \sin B = \frac{1}{2}(\cos(A-B) - \cos(A+B))$$

when 2 frequencies are equal, but with different phase angles, eg. $A = 2\pi ft + \theta$ for signal V_x & $B = 2\pi ft$ for signal V_y.

$$[\sin(2\pi ft + \theta)][(\sin(2\pi ft))] = \frac{1}{2}[\cos\theta - \cos(4\pi ft + \theta)]$$

$$= \frac{1}{2}(dc - \text{the double frequency term})$$

$\therefore$ 2 i/p s/l V_x & V_y are applied to multiplier $V_o(dc)$

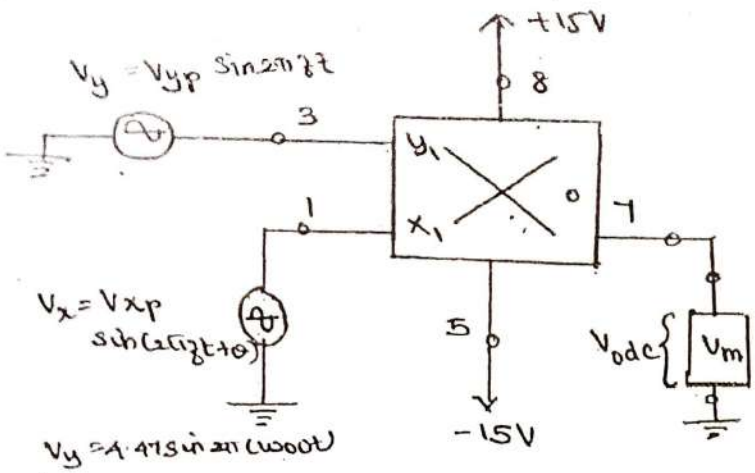
$$V_o(dc) = \frac{V_{xp} V_{yp}}{20} \cos\theta.$$

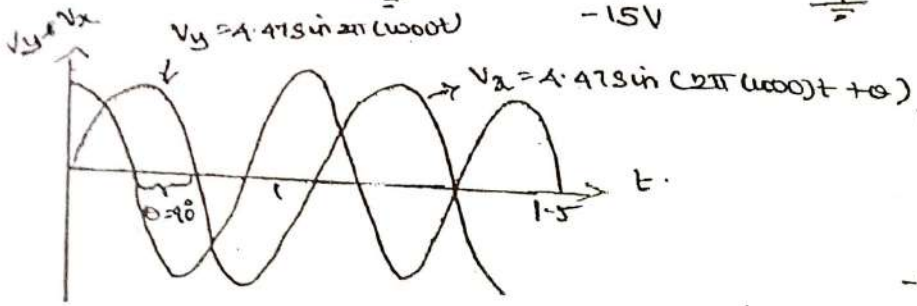
V_{xp} & V_{yp} = peak voltage amplitudes of s/l V_x & V_y.

$\Rightarrow$ $V_o(dc)$ depends on $\cos\theta$.

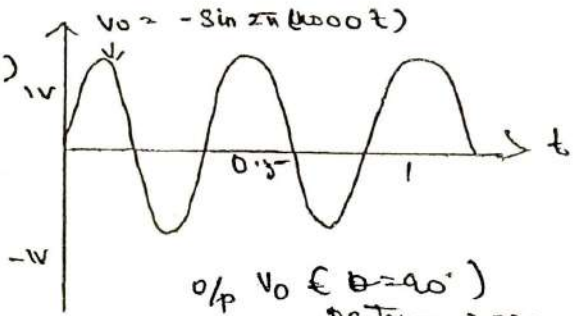
Dc voltmeter can be calibrated as phase angle meter when $V_{xp} * V_{yp}$ is equal to 20.

$V_{o(dc)} = \cos\theta$; when $V_{xp}\ V_{yp} = 20$ or $V_{xp} = V_{yp} = 14.14V$





θ = 90°



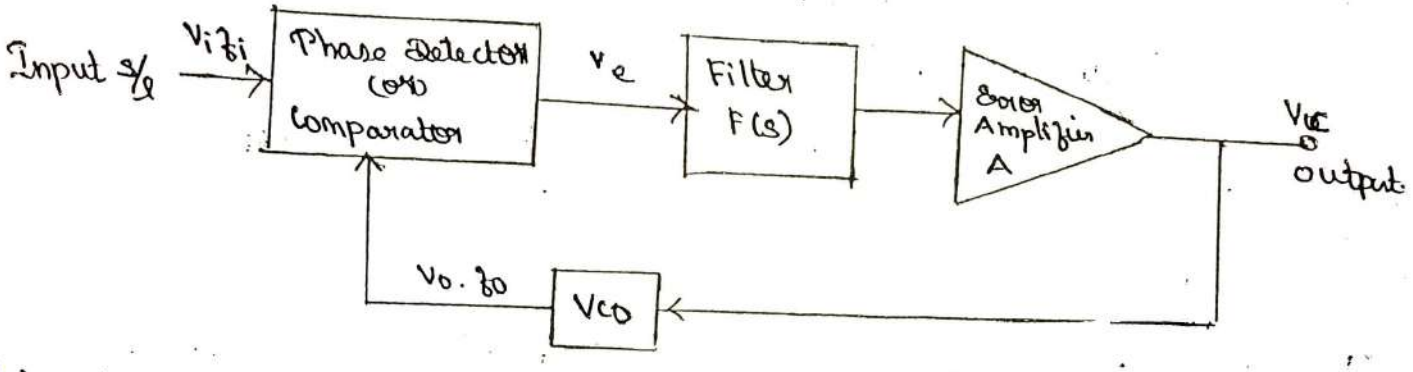
o/p V_o ∈ θ = 90°)
DC term = 0V

PHASE-LOCKED LOOP

APPLICATION:- Radar synchronisation & communication Application.
Satellite communication & electronic frequency control.
Air borne Navigation s/m.
FH communication s/m, computers etc.

BASIC PRINCIPLES & OPERATION OF THE BASIC PLL

Block diagram of basic PLL is.



Main elements :-

- → Phase Detector / comparator
- → LPF
- → Error Amplifier
- → VCO ⇒ Voltage Controlled Oscillator.

Phase Detector :- It is a multiplier which generates sum & difference of 2 i/p signals.

Free running frequency f_o of the VCO is determined by externally connected resistor & a timing capacitor.

When loop is locked, frequency $f_o \propto$ to externally applied voltage V_c called dc control voltage.

Input periodic signal V_i of frequency f_i & VCO output signal V_o of frequency f_o are applied to PLL, Phase detector produce a dc or low frequency signal V_e which is ~~perpo~~ proportional to phase difference between V_i & V_o.

i.e, $V_e \propto$ (difference in phase V_i & V_o)

frequency sum components is filtered out.

Low frequency difference signal is passed out the filter & then amplified by error Amplifier (A).

This amplified signal is applied as input to VCO as control voltage V_c. which changes VCO frequency f_o in such a way difference between f_o & f_i is reduced.

When these two frequency is brought identical by this feedback action then circuit is said to be locked.

Once locked, $f_o = f_i$, with inzinite phase difference ϕ.

Process of Capture :-

[Process of capture]

Important aspect of PLL, by which loop achieves condition of being in-lock with signal from a free-running and unlocked condition.

In unlocked condition of PLL, VCO operate at f_c called "centre frequency or free running frequency". Coresponds to applied voltage of 0V dc at its control input. Capture process is non-linear.

Assume, feedback loop of PLL is initially open between loop-filter & VCO. control input.

Input signal frequency f_i assumed to be closer to VCO centre frequ f_c is applied to the input of the phase detector.

Phase detector, is usually ~~phase~~ detector analog. multiplier that multiplies two sinusoidal together. & produce sum & difference of i/p as its o/p.

High frequency sum components is filtered out by LPF & o/p of LPF is difference between VCO centre frequency f_c & incoming signal frequency f_i.

Consider that loop is closed, difference frequency is applied to VCO input as the control voltage V_c. This will make VCO frequency f_o, a sinusoidal frequency. function of time.

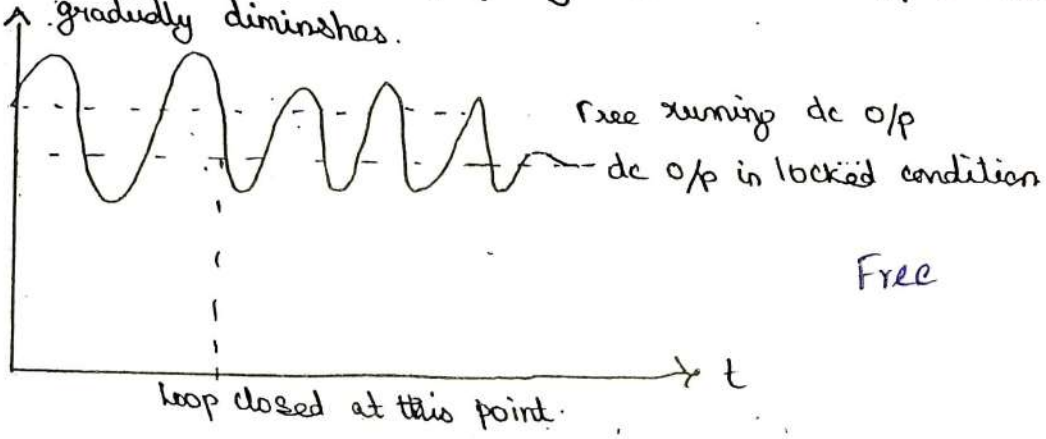
∴ It alternately moves "closer & farther" away from f_i.

O/p of phase detector ⇒ $f_o - f_i$ moves higher frequency when f_o moves away from f_i & moves to lower frequency when f_o moves closer to f_i

O/p of phase detector has asymmetrical wave shape during capture process. This produce dc component in phase detector O/p.

Dc component shifts the VCO frequency f_o towards f_i & thus frequency difference V_o gradually diminishes.

O/p of phase detector during capture process.



when loop is locked; frequency difference becomes zero. & dc voltage remain at the loop filter O/p.

LPF filter $f_o - f_i$ resulting from interfering signal, which are far away from f_o. It also acts as memory for loop., when lock is momentarily lost due to large interfering transient signal.

∴ Capture Range & Pull-in time are dependant on amount of Gain in the loop. & Bandwidth of the filter.

S/s will be out of capture range when boot frequency is too high due to VCO frequency which is far away from centre frequency.

Once locked achieved, VCO track signal well beyond capture-range.

~~Reduce~~ Reduce B.W of filter → improve rejecitivity of out of band s/s & ↓ capture range & pull in time ↑ res & loop phase margin (less)

Capture Range : Capture Range of PLL is defined as one range of input frequency around centre frequency within which the loop get locked from an unlocked condition.

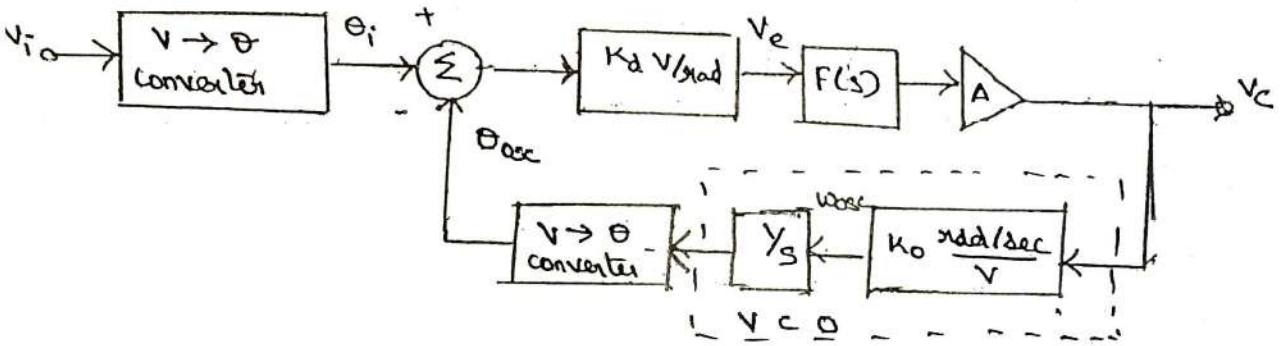
Pull-In-Time :- Pull-in Time is the total time required for the loop to get captured with input signal.

Important feature of PLL :- Ability to suppress the noise such as those superimposed on the input signal & noise generated by VCO.

Free running stage
capture range
Lock Range
Pull in time

LOOP ANALYSIS OF PLL:

closed



Assume PLL is initially in locked condition. Also assume, gain of the phase detector is K_d volt/rad of phase difference, Transfer characteristic of loop filter is F(s) & Gain of forward loop is A.

i/p sinusoidal s/s, V_i is $V_i = V_p \sin(\omega t + \theta_i)$ — (1)

If phase shift of the signal at the VCO o/p is θ_{osc}, the average value of the o/p of phase detector is

$$V_e = K_d (\theta_i - \theta_{osc}) \quad - (2)$$

θ_i & θ_{osc} = phase shift w.r.t an arbitrarily assumed reference.

Phase of the signal at the o/p of VCO as a function of time is Equal to integral of the VCO o/p frequency.

$$\omega_{osc}(t) = \frac{d\,\theta_{osc}(t)}{dt}$$

$$\theta_{osc}(t) = \int_0^t \omega_{osc}(t)\,dt + \theta_{osc}|_{t=0}$$

∴ integral component is represented as $1/s$ inside the VCO block.

Oscillator frequency ω_{osc} & dc control voltage V_c is related

$$\omega_{osc} = \omega_c + K_0 V_c \qquad -(3)$$

ω_c = centre or free-running angular frequency when $V_c = 0$ & K_0 is VCO Gain in rad/s per volt.

Closed-loop transfer function of the PLL becomes.

$$\frac{V_c(s)}{\theta_i(s)} = \frac{K_d F(s) A}{1 + K_d A F(s) \frac{K_0}{s}}$$

$$= \frac{s K_d F(s) A}{s + K_d K_0 A F(s)} \qquad -(4)$$

Response of the loop to frequency variation at the i/p rather than phase,

$$\frac{V_c(s)}{\omega_i(s)} = \frac{V_c(s)}{s\theta_i(s)} = \frac{K_d F(s).A}{s + K_d K_0 A F(s)} \qquad -(5)$$

$\omega_i = d\theta_i/dt$, $\omega_i(s) = s\theta_i(s)$

consider $F(s) = 1$; 1st order LPF.

$$\frac{V_c(s)}{\omega_i(s)} = \frac{K_v}{s + K_v} \times \frac{1}{K_0} \qquad -(6)$$

K_v = Loop bandwidth , $K_v = K_0 K_d \cdot A$

K_v = effective bandwidth of loop & Capture range depent on K_v. If K_v decreare, capture time rises & capture-range reduces. ∴ property of interference rejection improves.

Second-order PLL :-

1st order PLL has several limitation.

→ Both sum & difference frequency component are fed to the o/p from Phase detector.

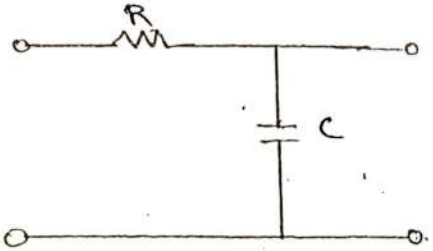
→ All out of band interfering signals from the i/p will appear shifted in frequency at the o/p

Loop-filter is highly desirable in application where interfering S/s are present.

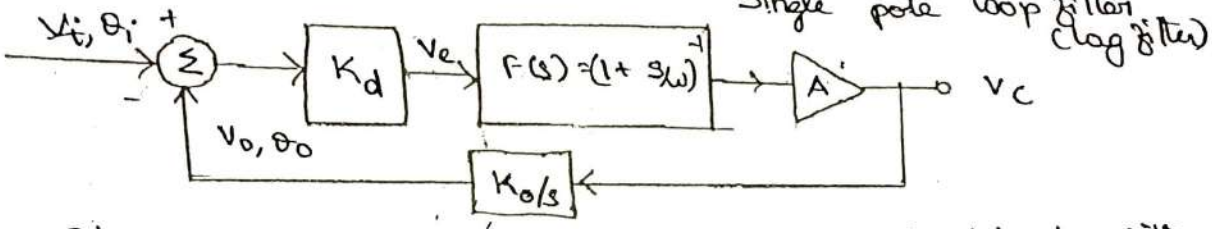
Common configuration of monolithic PLL is 2nd order loop with loop filter $F(s)$ of simple single-pole, low pass filter realized with R & C

$$F(s) = \frac{1}{1+s/\omega} = \frac{1}{1+s\tau} \quad - (7)$$

$$\omega = 1/RC = 1/\tau$$



Single pole loop filter (Lag filter)



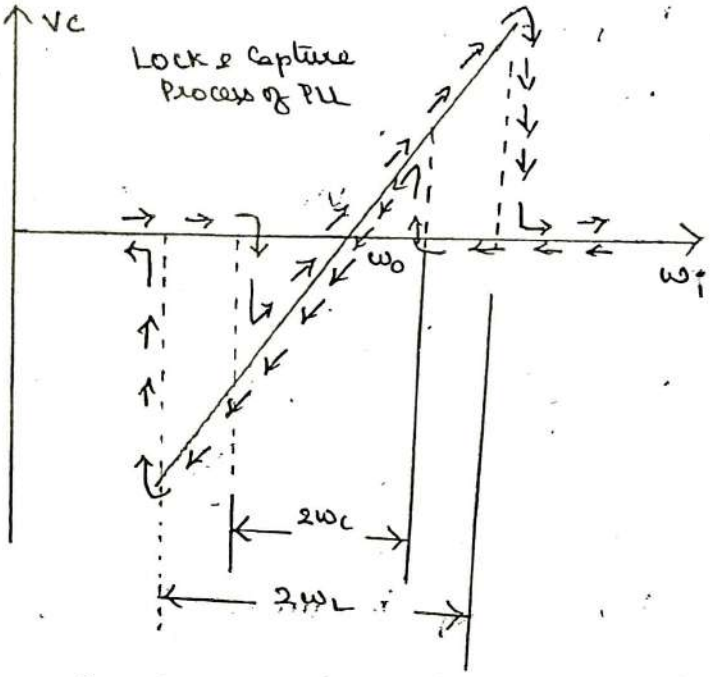
Block Diagram of Second-order PLL using single pole loop filter.

Loop lock-range & Capture Range :-

Loop lock-range is represented as the range of frequencies about ω_o for which the PLL maintains the relationship $\omega_i = \omega_{osc}$.

If phase detector can determine the phase difference between θ_i & θ_{osc} over a $\pm \pi/2$ range;

lock-range is,



$$\omega_L = \pm \Delta\omega_{osc}$$
$$= K_d A K_o (\pm \pi/2)$$
$$= \pm K_v (\pi/2) \quad - (8)$$

Capture Range is range of i/p frequencies within which an initially unlocked loop will get locked with an i/p S/g.

$F(s) = 1$; capture range = lock-range.

If $F(s) = \frac{1}{(1+s/\omega_i)}$ $\Rightarrow$ Capture range < lock range.

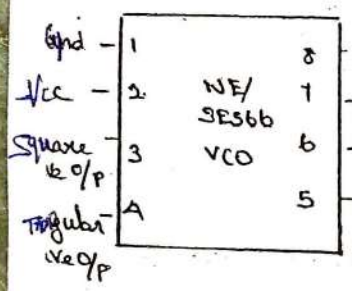
VOLTAGE CONTROLLED OSCILLATOR: [VCO]

* VCO is an oscillator whose oscillating frequency varies in response to control voltage V_c. $\Rightarrow f_0 = KV_c$ $\Rightarrow V_c > 0$ & K is defined as sensitivity of VCO in rad/volt.

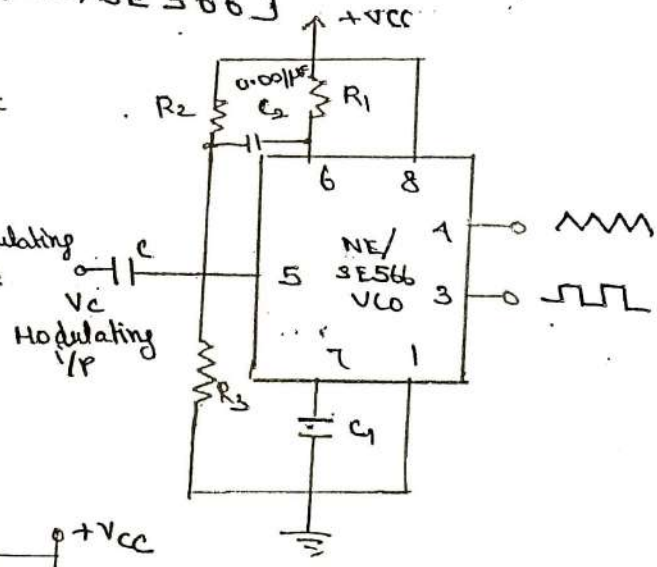
Properties:-

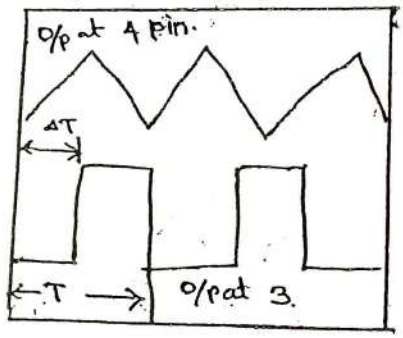
- → Linearity in voltage to frequency conversion.
- → Frequency stability against temperature changes & drift characteristics
- → High operating frequency & wide tracking range of frequencies.
- → High Modulation sensitivity K_0 & ease of tuning.

IC 566 VCO :- [NE/SE 566]

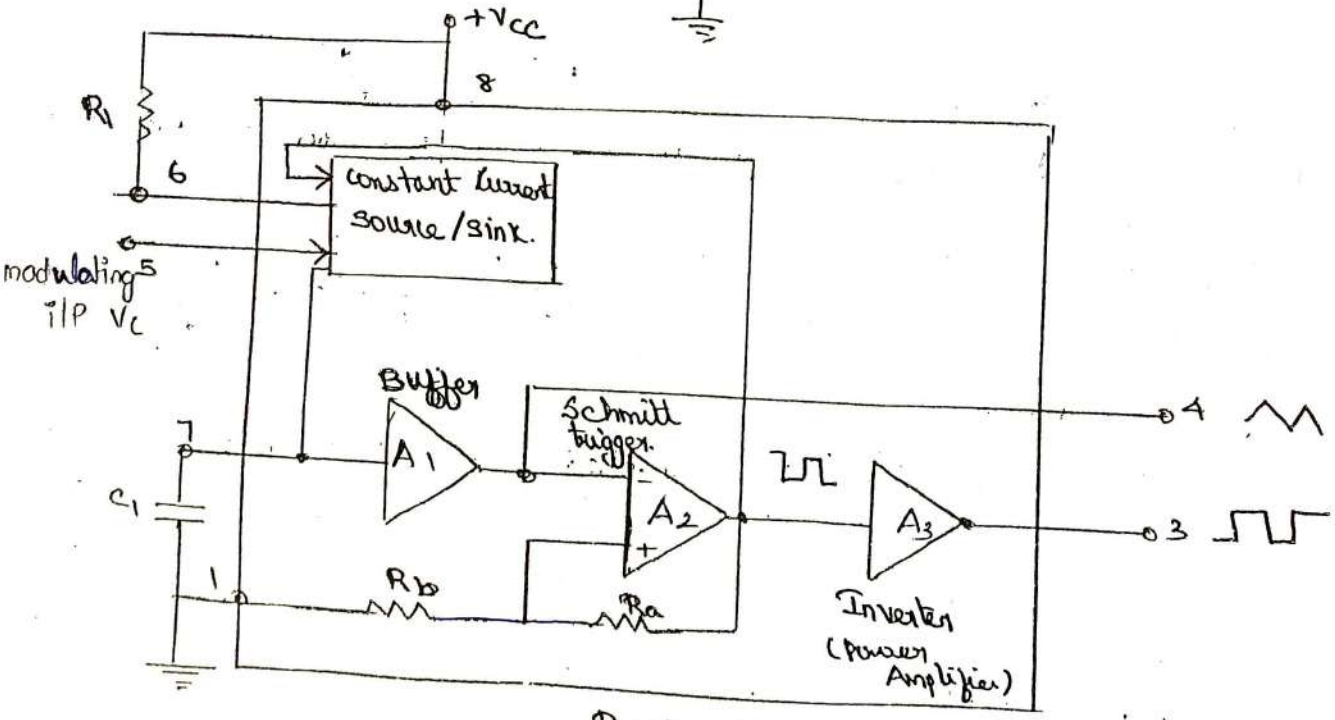


Pin diagram.





o/p wave form



Basic Block Diagram.

The frequency of oscillation is determined by an externally connected resistor R_1 & capacitor C_1.

Control voltage or modulating input V_c is applied at control terminal (pin 5).

Triangular voltage obtained at pin 4 is applied. It is generated by alternately charging capacitor C_1 by one current source, & discharging it linearily through another current source.

Amount of charge & discharge voltage swing is determined by schmitt trigger. It provide square-wave o/p at pin 3 through power amplifier A_3. & triangular-wave o/p at pin 4 through buffer amplifier A_1

Operation of VCO :-

o/p voltage swing of the schmitt trigger is set to level V_{cc} & $0.5V_{cc}$ If $R_a = R_b$ in positive feedback path. voltage at non-inverting terminal of A_2 swings from $0.5V_{cc}$ to $0.25V_{cc}$.

During charging of C_1, voltage across C_1 just exceed $0.5V_{cc}$, schmitt trigger switches to LOW ($0.5V_{cc}$) & capacitor starts discharging. When voltage across C_1 reduces to $0.25V_{cc}$ the schmitt trigger switches to HIGH (V_{cc})

Maintain source current & sink current equal to obtain equal +ve & -ve slope. at pin 4.

Square-wave o/p of schmitt trigger, inverted & buffered at pin 3.

Calculation of free Running frequency f_0 of VCO :

Voltage change across capacitor C_1 is $\Delta V = 0.25V_{cc}$. Since constant current source are used, rate of change of voltage across the capacitor is given by

$$\frac{\Delta V}{\Delta t} = I/C_1$$

$$\frac{0.25V_{cc}}{\Delta t} = \frac{i}{C_1}$$

$$\Delta t = \frac{0.25V_{cc} \cdot C_1}{i} \rightarrow (1)$$

Time period T of the triangular waveform is $2\Delta t$.

∴ frequency of oscillation f_0 is

$$f_0 = \frac{1}{T} = \frac{1}{2\Delta t} = \frac{i}{0.5V_{cc}C_1} \rightarrow (2)$$

$$i = \frac{V_{cc} - V_c}{R_1} \quad ; V_c = \text{voltage at pin 5.} \rightarrow (3)$$

$$f_0 = \frac{2(V_{cc} - V_c)}{C_1 R_1 V_{cc}} \rightarrow (4)$$

∴ O/p frequency of VCO varied by

→ External resistor R_1

→ External capacitor C_1

→ control voltage V_c applied at pin 5.

Voltage V_c at pin 5 is set by voltage divider circuit consisting of R_2 & R_3. If V_c is initally set to $\frac{7}{8}V_{cc}$, then.

$$f_0 = \frac{2(V_{cc} - (7/8)V_{cc})}{C_1 R_1 V_{cc}} = \frac{1}{4R_1C_1} = \frac{0.25}{R_1C_1} \rightarrow (5)$$

Voltage - to - frequency conversion factor:

The voltage - to - frequency conversion factor is determined by $K_v = \frac{\Delta f_0}{\Delta V_c}$

ΔV_c = change in modulating signal required to produce a corresponding shift Δf_0 in frequency. Assuming centre frequency is f_0 & new frequency f_1

$$\Delta f = f_1 - f_0.$$

$$= \frac{2(V_{cc} - V_c + \Delta V_c)}{C_1 R_1 V_{cc}} - \frac{2(V_{cc} - V_c)}{C_1 R_1 V_{cc}}$$

$$\Delta f = \frac{2\Delta V_c}{C_1 R_1 V_{cc}}$$

$$\frac{\Delta f}{\Delta V_c} = K_V = \frac{2}{C_1 R_1 V_{cc}}$$

$$f_0 = \frac{1}{4 R_1 C_1}$$

$$K_V = \frac{8 f_0}{V_c}$$

MONOLITHIC PHASE-LOCKED LOOP:
[MONOLITHIC PHASE LOCKED LOOP]

* Monolithic PLLs are SE/NE 560 series from signetics - LM560 series from National semiconductor corp.

* PLL circuit consist of a Gilbert type phase detector, temperature-compensated VCO & facility for connecting an external RC circuit to perform the loop-filter function.

IE 565 PLL:

The analog phase detector circuit of PLL comprises of Q_1-Q_2, Q_3-Q_4 & Q_5-Q_6 differential amplifier pairs.

Q_{37} & R_3 serve as current-sink bias source.

R_1 & R_2 serve as loads for the phase detector. The diode connected transistors Q_7 & Q_3 reduce the voltage swings to $\pm 0.7V$ & conversion ratio of PLL becomes

$$K_d = \frac{0.7-(-0.7)}{\pi} = \frac{1.4}{\pi} \quad -(1)$$

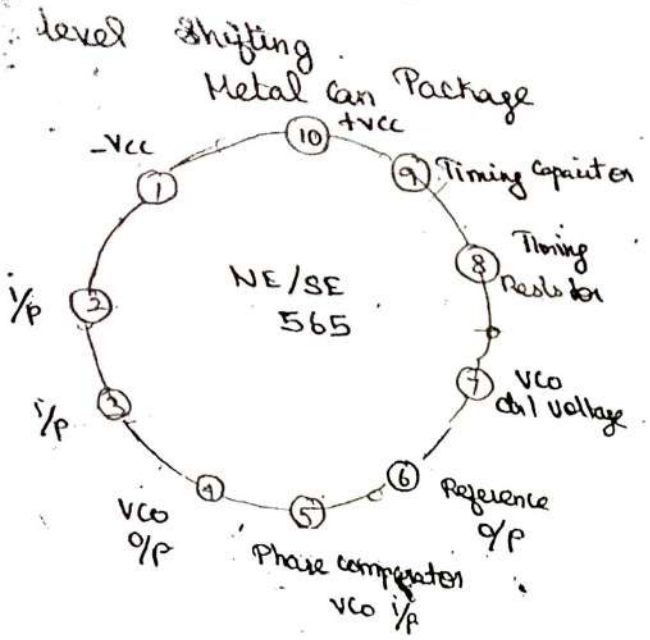
Balanced O/P from the phase detector is supplied to the differential transistor pair Q_{10}, Q_{11} biased by Q_{39} which acts as the current sink. This stage works for a gain of 1.4 & a single ended O/P from this stage taken across R_{12}.

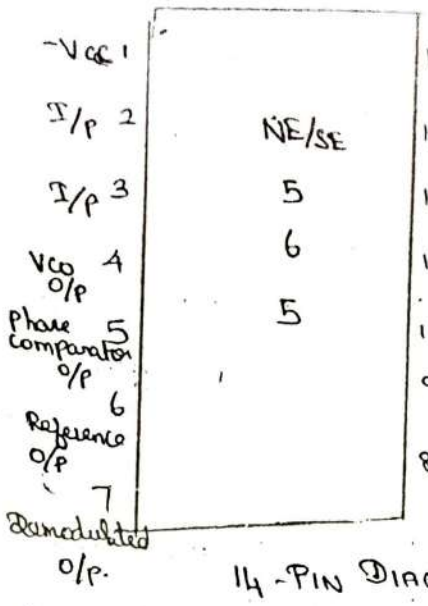
Resistor R_{12} in combination with the external capacitor connected between pin 7 & ground form the loop-filter.

Transistors Q_{12} through Q_{23} form the voltage controlled current source for the VCO. Equal charging & discharging currents are supplied to the external capacitor C_1 connected to pin 9. Resistor R_1 is connected between pin 8 & $+V_{CC}$.

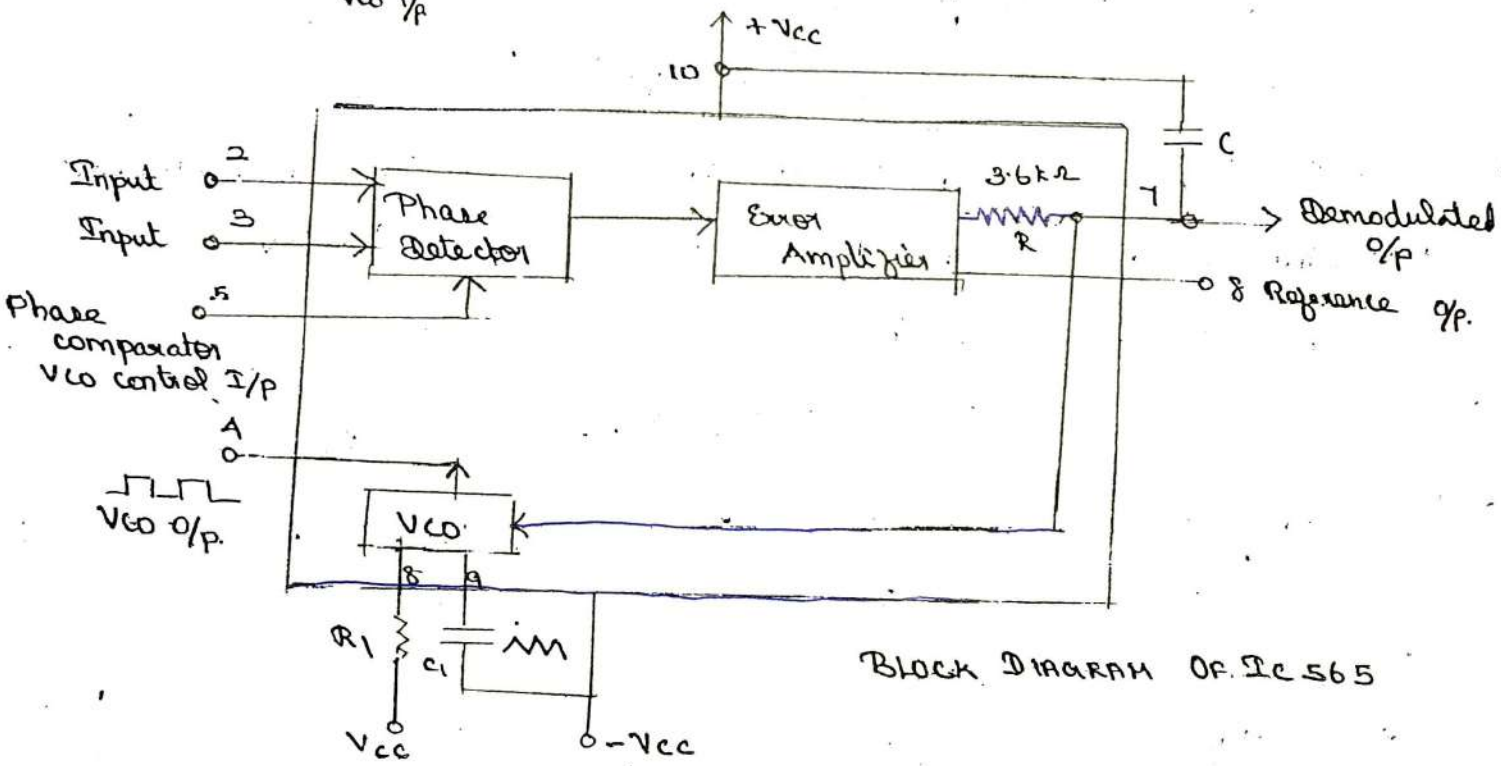
Schmitt trigger formed by Q_{25} through Q_{36} with differential amplifier O/P circuit consisting of Q_{33} & Q_{34} from part of VCO. Charging & discharging cycles through the current source are determined by switching the transistor Q_{23} & Q_{24} ON or OFF

Transistor Q_{14}, Q_{26}, Q_{30} & Q_{35} connected as diodes generate the desired level shifting.





14-PIN DIAGRAM



BLOCK DIAGRAM OF IC 565

IC 565 is available in 14 pin DIP package & 10-pin Metal can Package.

O/p of phase detector is applied to a differential amplifier

Single ended o/p dropped across R is connected internally to VCO. It is also demodulated o/p at pin 7 of PLL.

R is part of LPF. Capacitor C between pin 7 & 10 along with the internal resistor, R of 3.6kΩ form the LPF. Capacitor C should be large enough to eliminate variation in demodulated o/p voltage at pin 7.

Dual power supply ±6V to ±12V, & single supply +12V & +24V.

rating characteristics :- Voltage = ±6V & $T_A = +25°C$

0.001μF C is connected between pin 7 & 8. to avoid oscillations due to parasitic effect.

Free running or centre frequency of VCO is

$$f_0 = \frac{1.2}{4R_1C_1} \quad -(2)$$

R_1 & C_1 = External Resistor & capacitor. connected to pin 8 & 9.

R_1 ⇒ 2KΩ to 20KΩ

Device can achieve lock with an i/p signal over ±60% of B.W w.r.t f_0.

Pin 2 & 3 two i/p terminal of IC 565. The i/p S/A can also be direct coupled without any dc voltage difference between the pins, dc resistance from pin 2 & 3 being equal.

Derivation of Lock-in-Range :-

* Assume ϕ radians is the phase difference between i/p S/a & VCO Voltage. O/p of phase detector V_e is

$$V_e = K_d(\phi - \pi/2) \quad -(3)$$

K_d = Phase angle-to-voltage transfer co-efficient of phase detector.

control voltage at VCO is $V_c = AK_d(\phi - \pi/2) \quad -(4)$

A = Voltage Gain of Amplifier.

VCO shifts free running frequency f_0 to frequency f is

$$f = f_0 + K_0V_c \quad -(5)$$

K_0 = Voltage to frequency transfer coefficient of VCO.

PLL achieve lock with signal frequency f_i

$$f = f_i = f_0 + K_0V_c \quad -(6)$$

From (4) & (6)

$$V_c = \frac{f_i - f_0}{K_0} = AK_d(\phi - \pi/2) \quad -(7)$$

$$\phi = \pi/2 + (f_i - f_0)/K_0K_dA \quad -(8)$$

maximum o/p voltage magnitude available from the phase detector occurs for $\phi = \pi$ & 0 radian.

$$V_{c(max)} = \pm K_d \frac{\pi}{2}$$

∴ Maximum control voltage to drive VCO is

$$V_{c(max)} = \pm \left(\frac{\pi}{2}\right) K_d \cdot A \quad \text{—} \quad (9)$$

Maximum VCO swings in frequency that can be achieved is

$$(f - f_0)_{max} = K_0 V_{c(max)} = K_d K_0 A (\pi/2) \quad -(10)$$

∴ Maximum range of signal frequencies over which PLL can remain locked

$$f_i = f_0 \pm (f - f_0)_{max} \quad -$$

$$= f_0 \pm K_d K_0 A \left(\frac{\pi}{2}\right) = f_0 \pm \Delta f_L \quad - (11)$$

Lock in frequency range is $2\Delta f_L$ & from (11) it is given by

$$\text{Lock-in-range} = 2\Delta f_L = K_d K_0 A \pi = K_v \pi \quad - (12)$$

where $K_v = K_0 K_d A$. loop bandwidth.

or

$$\Delta f_L = K_d K_0 A \left(\frac{\pi}{2}\right) = K_v (\pi/2) \quad - (13)$$

Lock in range is symmetrically located with respect to free running frequency f_0 of VCO. IC PLL 565,

$$K_v = \frac{8 f_0}{V}$$

$$V = +V_{cc} - (-V_{cc})$$

$$K_d = \frac{1.4}{\pi}$$

$$A = 1.4.$$

$$\Delta f_L = \pm 7.8 \frac{f_0}{V} \quad -(14)$$

Derivation of capture range :

when PLL is not initially locked to the signal, the frequency of the VCO will be its free running frequency f_0.

Phase angle difference between the i/p signal & V.C.O output voltage will be.

$$\phi = (\omega_i t + \phi_i) - (\omega_0 t + \phi_0)$$

$$= (\omega_i - \omega_0) t + \Delta\theta \quad - (15)$$

Thus phase difference is not constant change with time.

$$\frac{d\phi}{dt} = \omega_i - \omega_0 \quad - (16)$$

Phase detector output voltage will therefore not have a dc component but will produce ac voltage with a triangular waveform of peak amplitude $K_d(\pi/2)$ & fundamental frequency $(f_i - f_0) = \Delta f$.

LPF is simple RC network ; T.F $\Rightarrow T(f) = \frac{1}{1 + j(f/f_1)}$ - (17)

i/p to LPF :

$$\Delta f = f_i - f_0 ,$$

$\Delta f > 3f_1$, L.P.F T.F will be

$$T(\Delta f) = \frac{f_1}{\Delta f} = \frac{f_1}{f_i - f_0} \quad - (18)$$

voltage V_c to drive VCO

$$V_c = V_e \times T(f) \times A$$

$$V_{c(max)} = V_{e(max)} \times T(f) \times A \quad - (19)$$

w.k.T $\quad V_{c(max)} = \pm K_d (\pi/2) A (f_1/\Delta f)$

Corresponding value of maximum VCO frequency shifts is

$$(f - f_0)_{max} = K_0 V_{c(max)}$$

$$= K_d K_0 (\pi/2) \cdot A \cdot (f_1/\Delta f) \quad - (20)$$

let $f_i = f$, for acquisition of signal frequency, maximum signal frequency range that can be acquired by PLL is

$$(f_i - f_0)_{max} = \pm K_d K_0 \left(\frac{\pi}{2}\right) A (f_1/\Delta f_c) \quad - (21)$$

$$\Delta f_c = (f_1 - f_0)_{max}$$

$$(\Delta\omega_c)^2 = K_d K_0 \left(\frac{\pi}{2}\right) A \omega_1$$

since $\Delta\omega_L = \pm K_d K_0 \left(\frac{\pi}{2}\right) A$; we get

$$\Delta\omega_c = \pm\sqrt{\omega_1 \Delta\omega_L} \quad \rightarrow (22)$$

Total capture range is

$$2\Delta\omega_c \simeq 2\sqrt{\omega_1 \Delta\omega_L}$$

here lock-in range $= 2\Delta\omega_L = K_d K_0 A\pi = K_v\pi$.

IC 565, R = 3 kΩ

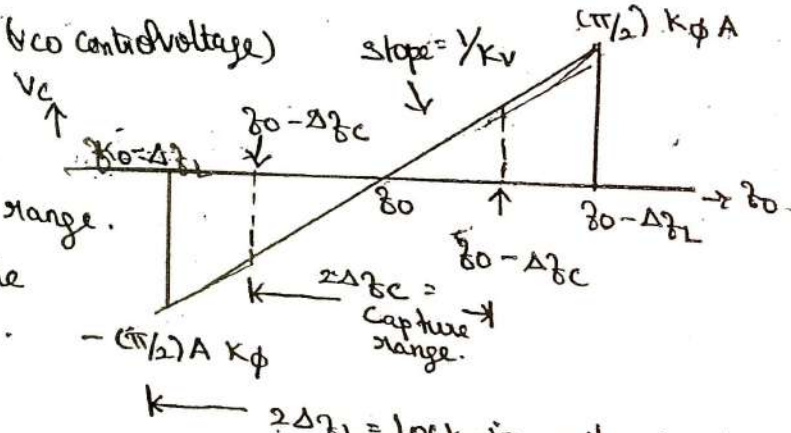
$$\therefore \Delta\omega_c = \pm\left[\frac{\Delta\omega_L}{(2\pi)(3.6\times10^3)\,C}\right]^{1/2} \rightarrow (23)$$

C = Farads.

Capture Range is symmetrically located w.r.t ω_0 of VCO.

PLL cannot obtain lock outside capture range.

Once captured, it will hold on until the signal frequency goes beyond the lock-in range.



To increase lock-in range, larger capture range, is required

If Capature-range is increased, PLL susceptible to noise. LPF bandwidth is reduced to minimize interference.

1) For PLL 565, given the free-running freq as 100KHz, the demodulation capacitor of 2μF and supply voltage is ±6V determine the lock & capture freq. & identify the component values.

Soln $f_0 = 100KHz$, $C = 2\mu F$, $V_{cc} = \pm 6V$

$$\therefore \Delta f_L = \pm \frac{7.8 f_0}{V} = \pm \frac{7.8 f_0}{V_{cc} - (-V_{cc})} = \pm \frac{7.8 \times 100 \times 10^3}{6-(-6)}$$

$$= \pm 65 KHz$$

$$\therefore 2\Delta f_L = 2 \times 65KHz = 130KHz.$$

$$\Delta f_c = \pm \sqrt{\frac{\Delta f_L}{2\pi \times 3.6 \times 10^3 \times C}} = \pm \sqrt{\frac{65 \times 10^3}{2\pi \times 3.6 \times 10^3 \times 2 \times 10^{-6}}}$$

$$= \pm 1.199 KHz$$

$$f_0 = \frac{1.2}{4R_1C_1}$$

assume, $R_1 = 12K\Omega$. a standard value

$$100 \times 10^3 = \frac{1.2}{4 \times 12 \times 10^3 \times C_1}$$

$$\therefore C_1 = \frac{1.2}{4 \times 12 \times 10^3 \times 100 \times 10^3} = 25 \times 10^{-10} F$$

$$= 250pF.$$

2) Determine the output freq. f_0, lock range Δf_L and capture range Δf_c of IC 565. Assume $R_1 = 15K\Omega$, $C_1 = 0.01\mu F$ & $C = 1\mu F$ & $V_{cc} = +12V$.

Soln :

$R_1 = 15K\Omega$, $C_1 = 0.01\mu F$ & $C = 1\mu F$

$\therefore$ free running freq. $f_0 = \frac{1.2}{4R_1C_1}$

$$= \frac{1.2}{4 \times 15 \times 10^3 \times 0.01 \times 10^{-6}} = 2KHz$$

Lock range $= \Delta f_L = \frac{\pm 7.8 f_0}{V}$

$= \pm \frac{7.8 \times 2000}{12} = \pm 1.3 KHZ$

Capture range.

$$\Delta f_C = \pm \left[\frac{\Delta f_L}{2\pi (3.6 \times 10^3) \times C} \right]^{1/2}$$

$$= \pm \left[\frac{1.3 \times 10^3}{2 \times \pi \times 3.6 \times 10^3 \times 1 \times 10^{-6}} \right]^{1/2}$$

$= 239.73 HZ.$

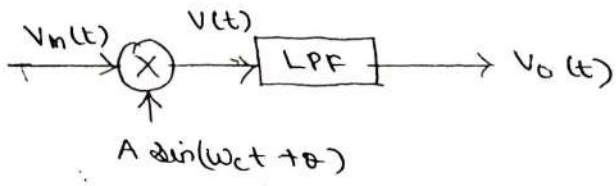
UNIT - III

AM Detection:

* PLL can be used as an AM detector for demodulating the amplitude modulated signals. Assume AM signal is given by

$$V_m(t) = V_p[1 + m(t)] \sin \omega_c t = V_p + V_p m(t) \sin \omega_c t$$

: Signal $V_m(t)$ can be demodulated by multiplying the signal with a local oscillator signal of the same carrier frequency f_c.



Simple AM detector.

Then multiplier o/p is

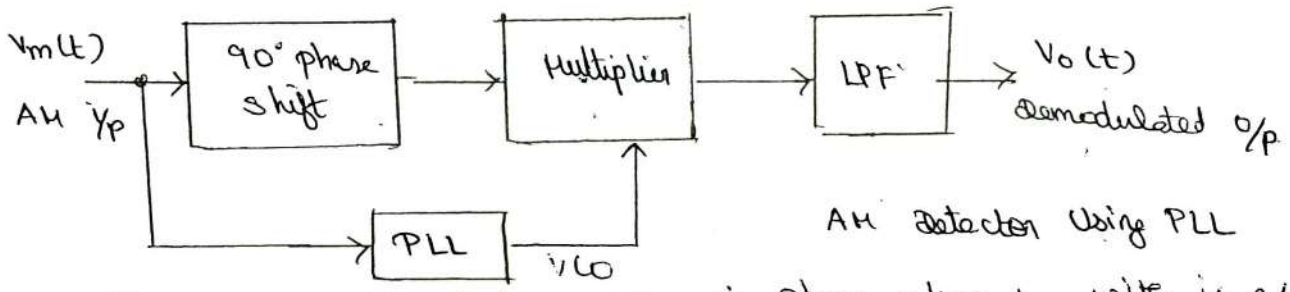
$$V_o(t) = AV_p[(1 + m(t)] \sin \omega_c t \sin(\omega_c t + \theta))]$$

$$= AV_p[1 + m(t)] \frac{\cos\theta - \cos(2\omega_c t + \theta)}{2}$$

* High-frequency 2nd term can be removed by LPF and hence filter o/p becomes

$$V_o(t) = V[1 + m(t) \cos\theta]$$

$V = AV_p$



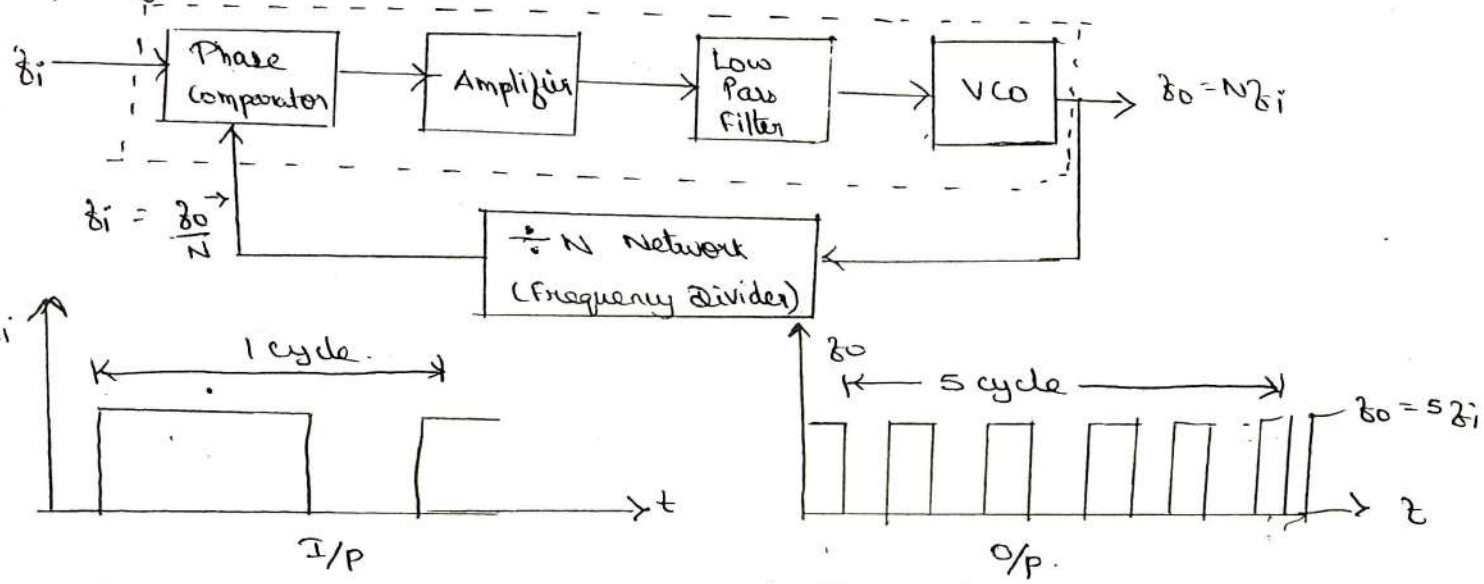
AM detector using PLL

* Local oscillator s/g generated in PLL in phase-locked with i/p s/g.
* PLL is locked to carrier frequency of amplitude modulated signal.
* VCO o/p of PLL, which has same frequency values as the carrier, but unmodulated, is applied as one i/p to the multiplier.
* In unlock condition, VCO o/p signal of PLL is 90° out of phase with the i/p signal.
* AM i/p signal is phase-shifted by 90° before being applied to the multiplier
* Two signals applied to multiplier, AM s/g & carrier s/g generated in PLL are now in phase.
* O/p of multiplier is then passed through LPF for removal of high frequency components.

APPLICATIONS OF IC 565 PLL

1. → Frequency Multiplication / Division
2. → AM Detection
3. → FM Detection
4. → FSK Modulation / Demodulation
5. → Frequency Synthesizing

Frequency Multiplication / Division :-



A Divide-by-N-network (frequency divider) is inserted between VCO and phase detector.

When PLL is in locked condition, O/P of frequency divider network is same as I/P frequency f_i.

VCO actually provides multiple of I/P frequency. This multiplication factor is achieved by inserting suitable divide-by-N network, N is integer.

In locked condition, $f_o = Nf_i$ Eg:: Divide-by-5 N/w shown.

Frequency Multiplication can also be obtained by operating PLL in harmonic locking mode for I/P signals, which is rich in harmonic such as square-wave.

Then VCO can get directly locked on the n^{th} harmonic of I/P signal without use of frequency divider. Value of n is limited to 10.

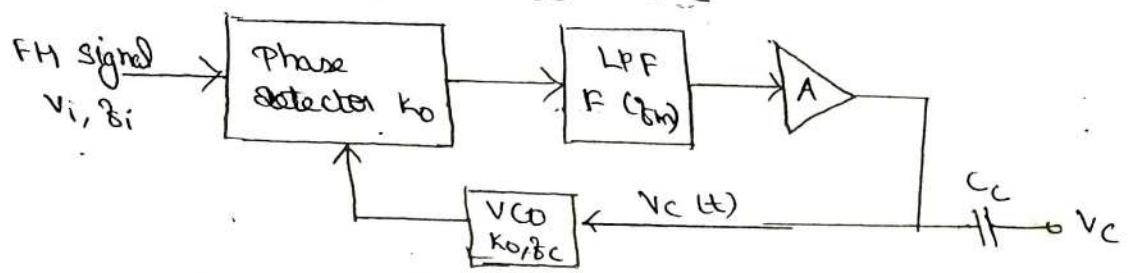
$V_o \propto$ Amplitude of i/p s/l

* This AM detector exhibits a high degree of selectivity due to the fact that PLL responds selectively to the carrier frequencies, which are very close to VCO o/p. Due to coherent detection, high degree of noise immunity.

FH Detection:

* PLL is set locked with the i/p FH signal. Then the VCO frequency will be equal to the instantaneous frequency of FH signal $f_i(t)$

$$f_i(t) = f_c + K_o V_c$$



* VCO control voltage V_c is demodulated FH o/p & $V_c = \frac{f_i(t) - f_c}{K_o}$

Error voltage controls the VCO to maintain lock with the i/p signal.

* The instantaneous frequency of the FH signal is given by

$$f_i(t) = f_c + \Delta f_c \sin \omega_m t$$

f_c = Carrier frequency, Δf_c = peak frequency deviation,

ω_m = angular frequency of the modulating s/l

AC Component of $V_c(t)$ after the capacitor C_c is

$$V_c(t) = \frac{f_i(t) - f_c}{K_o} = \frac{f_c + \Delta f_c \sin \omega_m t - f_c}{K_o}$$

$$V_c(t) = \Delta f_c \sin \omega_m t / K_o$$

This gives the modulating signal voltage applied to FH carrier at the transmitter

* Control voltage of VCO is a linear function of the instantaneous frequency deviation

* FM signal is demodulated, almost without any distortion.

∴ PLL can be employed for detection of wideband or narrowband FM s/l

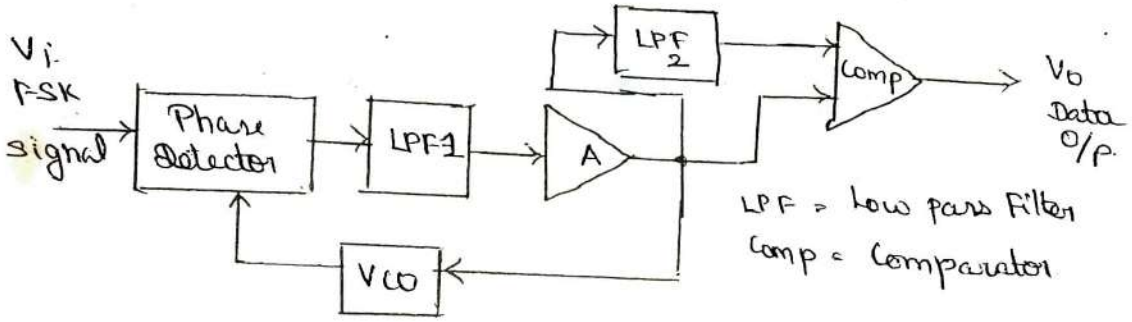
with higher degree of linearity, which cannot be achieved by any other detection methods.

* Centre frequency f_0 should be set as close as possible to FM carrier frequency f_c to achieve maximum symmetrical lock-range.

FSK Modulation / Demodulation :-

FSK is type of frequency modulation, in which binary data or code is transmitted by means of a carrier frequency that is shifted between two fixed frequency values, f_1 = logic 0, f_c = logic 1.

* Frequencies corresponding to logic 1 & logic 0 ⇒ mark & space.



* PLL is designed to remain in-lock with the FSK signal for both the frequencies f_1 & f_2. Then VCO control voltage fed to the comparator is given by

$$V_{f1} = \frac{f_1 - f_0}{K_0} \qquad V_{f2} = \frac{f_2 - f_0}{K_0}$$

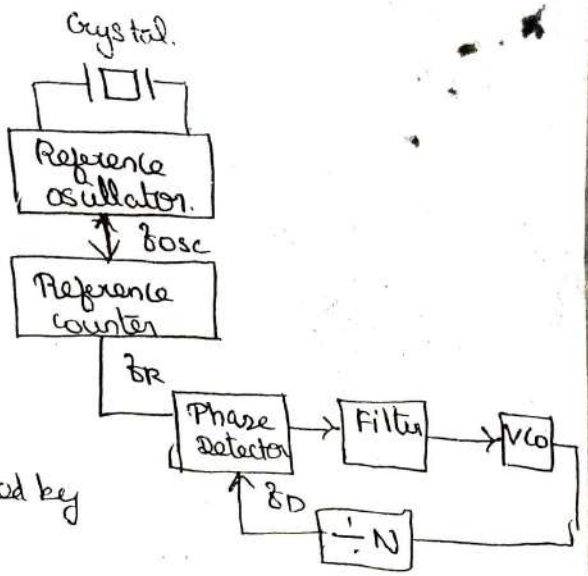
$$\Delta V_f = \frac{f_2 - f_1}{K_0}$$

- V_{f1} & V_{f2} applied to comparator, one i/p pass through LPF-2. Filter designed for time constant which is longer than FSK pulse duration to obtain a dc voltage.
- This dc voltage will have value mid way between V_{f1} & V_{f2}
FSK s/l V_i is applied to i/p, loop gets locked to i/p frequency & tracks it in between 2 frequencies f_1 & f_2.

$$f_1 = \frac{1.45}{(R_A \| R_C + 2R_B)C} = 1270\,Hz \qquad f_2 = \frac{1.45}{(R_A + 2R_B)C} = 1070\,Hz$$

Frequency Synthesizing:-

* It produces a large number of precise frequencies which are derived from single reference source of frequency, such as stable crystal controlled oscillator.



* A Temperature controlled crystal oscillator provides stable reference frequency f_R & 2nd i/p signal to phase detector is provided by o/p of VCO.

* A $\div$ by N counter is used in loop. $\therefore f_D = f_0/N$, f_0 = o/p freq of VCO.

* In locked condition, $f_R = f_D$.

$$\therefore f_0 = N f_R$$

* Divide by N counter is realized by programmable divider, $\therefore$ It is possible to achieve multiples of reference frequency.

* Frequency Synthesizing can also be obtained by harmonic locking in which locking is achieved with harmonic of reference signal.

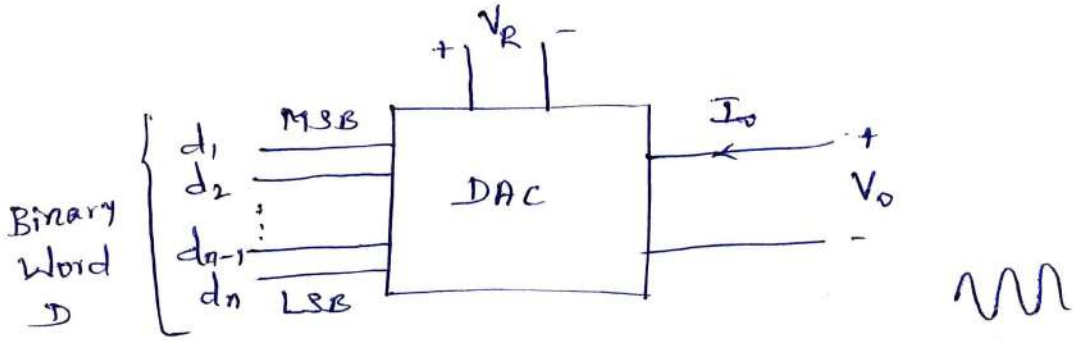
* VCO frequency is set to multiple of i/p reference frequency. The VCO locks with desired harmonic of i/p frequency.

Drawback:- lock-in range reduces when successively higher & weaker harmonics are used for locking.

UNIT-IV : ANALOG TO DIGITAL AND DIGITAL TO ANALOG CONVERTERS

ANALOG and DIGITAL DATA CONVERSIONS:

DIGITAL TO ANALOG CONVERTER [D/A CONVERTER (or) DAC]



Schematic of DAC

The input is an n-bit binary word D and is combined with a reference voltage V_R to give an analog output signal.

The output of a DAC can be either a voltage (or) current.

For a voltage output DAC, the D/A converter is mathematically described as,

$$V_o = k V_{FS} \left[d_1 2^{-1} + d_2 2^{-2} + \ldots + d_n 2^{-n} \right]$$

$V_o \rightarrow$ o/p voltage, $V_{FS} \rightarrow$ Full scale o/p vtg.

$k \rightarrow$ Scaling factor

$d_1, d_2, \ldots d_n \rightarrow$ n-bit binary Fractional word

$d_1 \rightarrow$ MSB

$d_n \rightarrow$ LSB

TYPES OF DIGITAL TO ANALOG CONVERTERS [DAC]

(i) Weighted resistor DAC

(ii) R-2R Ladder

(iii) Inverted R-2R Ladder

WEIGHTED RESISTOR TYPE D/A CONVERTER:

* In the weighted resistor type DAC each digital level is converted into an equivalent analog voltage or current.
* In a 4-bit DAC which accept data from 0000 to 1111 there are 15 discrete levels of input & hence it is convenient to divide the output analog signal into 15 levels.
* The LSB of the digital data causes a change in the analog output that is equal to $1/15^{th}$ of full-scale analog output voltage (V_R)

∴ the weighted resistor network is designed in such a way that a 1 in LSB (2^0) position results in $V_R \times \frac{1}{15}$ of o/p. A '1' in the 2^1 bit position must cause a change in the analog o/p voltage that is equal to $\frac{2}{15}^{th}$ of V_R (i.e, twice the size of LSB).

i.e, 1 in 2^2 $\Rightarrow V_R \times 4/15$ V

1 in $2^3 \Rightarrow V_R \times \frac{8}{15} V_R$

* Sum of the weights assigned to various bit position of a 4 bit DAC must be equal to 1 i.e, $(1/15 + 2/15 + 4/15 + 8/15) V_R = V_{FS}$
* In general, the weight assigned to the LSB is $\frac{1}{(2^n - 1)}$, where n = no. of bits in the digital input.

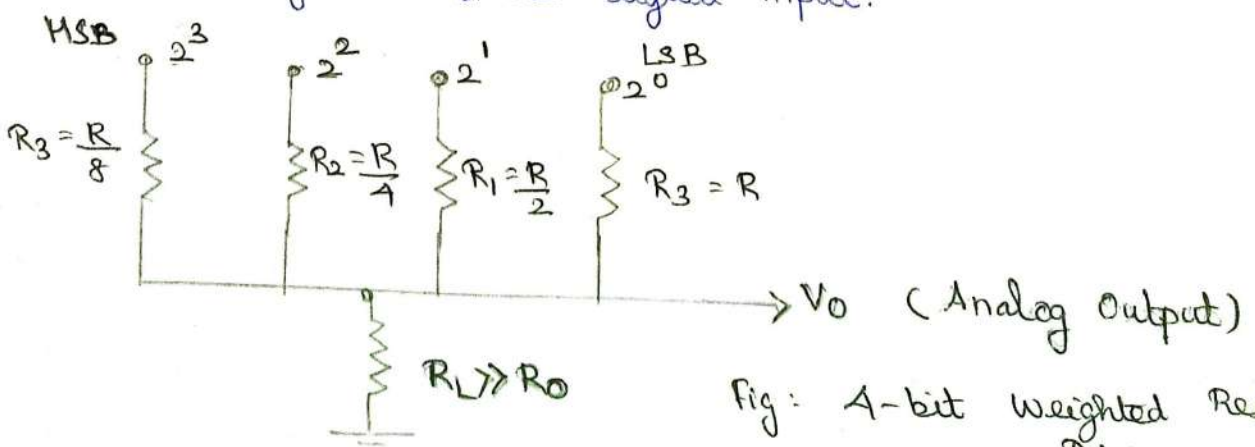


Fig: 4-bit Weighted Resistor DAC

1. The 2^0 bit is changed to $1/15^{th}$ of V_R, 2^1 bit to $2/15^{th}$ of V_R, 2^2 bit to $4/15^{th}$ of V_R & 2^3 bit to $8/15^{th}$ of V_R.

2. These 4 voltages are added together to form the analog output voltage using an op-amp summer circuit.

* The resistor R_0, R_1, R_2 & R_3 from the voltage divider network connected with the opamp and R_L is the load resistor which should be large enough so as not to load the divider network.

* LSB connected with highest i/p resistance R_0 while 2^1 bit is connected with a resistance of half the value of LSB resistor ie, $R_0/2$.

∴ its current contribution at the summing junction of op-amp will be twice that of LSB.

Hly 2^2 bit connected to $1/4^{th}$ of LSB resistance $= R_0/4$

2^3 bit " " $1/8^{th}$ of " " $= R_0/8$.

* O/p is the sum of these 4 attenuated voltages.

Operating Principle:

Illustration: The equivalent circuit, when applied with the digital data of 0001 is shown below.

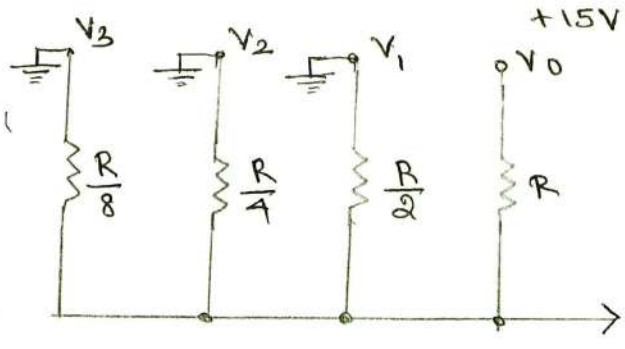


Fig: Equivalent circuit of a 4bit weighted resistor DAC for Input 0001

* The analog o/p voltage V_0 can be calculated using Millman's theorem, which states that the voltage at any node in a resistive network is equal to the sum of current entering the node

divided by the sum of the conductance connected at the node

Then O/p voltage is

$$V_0 = \frac{\frac{V_R}{R_1} + \frac{V_R}{R_2} + \frac{V_R}{R_3} + \frac{V_R}{R_4}}{1/R_1 + 1/R_2 + 1/R_3 + 1/R_4} \quad - (1)$$

* For the weighted resistor network, assuming $R_1 = R$, $R_2 = R/2$, $R_3 = R/4$ & $R_4 = R/8$ & apply Millman's theorem to the circuit, we get.

$$V_0 = \frac{\frac{V_R}{R} + \frac{V_R}{R/2} + \frac{V_R}{R/4} + \frac{V_R}{R/8}}{\frac{1}{R} + \frac{1}{R/2} + 1/R/4 + 1/R/8} \quad - (2)$$

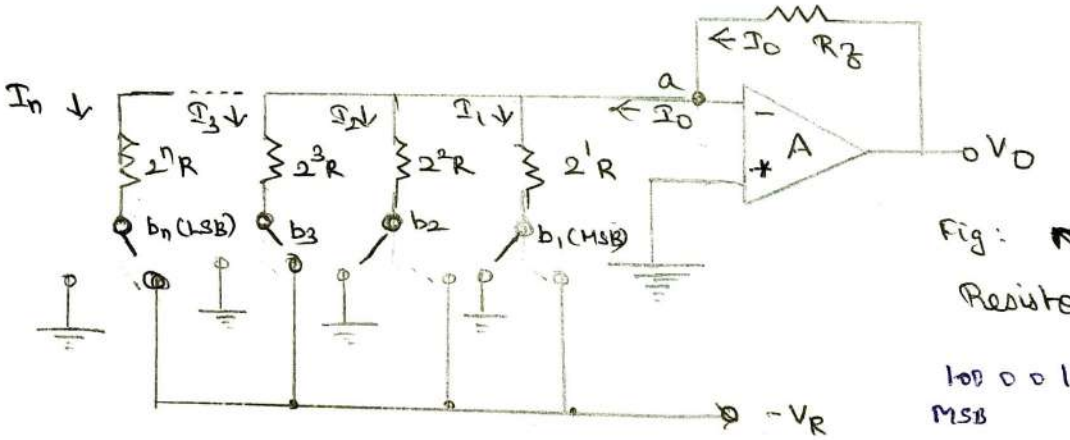


Fig: n-Bit Weighted Resistor DAC.

100 0 0 111
MSB LSB

* The above diagram is an n-bit DAC using op amp as a summing amplifier.
* It employs a binary weighted resistor network to generate the term $b_i 2^{-i}$ where $i = 1, 2 \ldots n$.
* The circuit also uses n - electronic switches controlled by the binary input word $b_1, b_2, \ldots b_n$ and reference voltage V_R.
* switches are of single pole double throw (SPDT) type.
* If binary i/p is 1, then switch connects to resistance to the reference voltage $-V_R$; if 0 → to Ground.

Considering an ideal opamp A, O/p current I_o is

$$I_o = I_1 + I_2 + \dots + I_n.$$

$$= \frac{V_R}{2^1 R} b_1 + \frac{V_R}{2^2 R} b_2 + \dots + \frac{V_R}{2^n R} b_n.$$

$$= \frac{V_R}{R} \left[b_1 2^{-1} + b_2 2^{-2} + \dots b_n 2^{-n} \right]$$

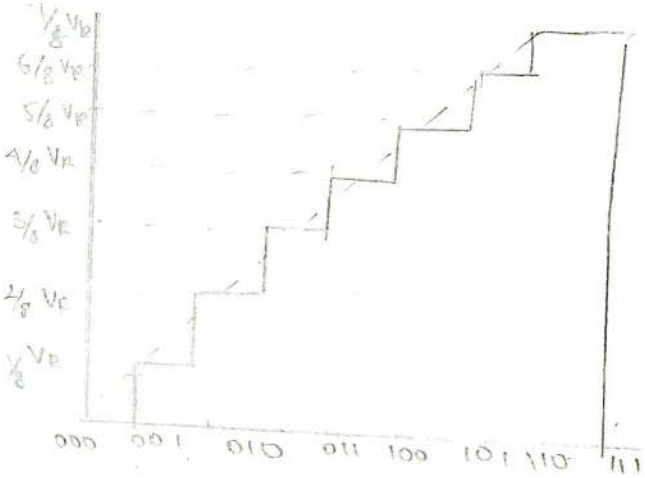
Then O/p voltage $V_o = I_o R_f$.

$$= \frac{V_R R_f}{R} \left[b_1 2^{-1} + b_2 2^{-2} + \dots + b_n 2^{-n} \right] - (3)$$

Using Eq: $V_o = K V_{FS} (b_1 2^{-1} + b_2 2^{-2} + \dots b_n 2^{-n})$ & (3).

it is seen that $R_f = R$, then $K = 1$, $V_{FS} = V_R$.

* The n-bit DAC ckt, uses a negative reference voltage, thus producing a positive staircase voltage.
* The analog O/p voltage waveform for 3-bit weighted resistor DAC is shown.



Transfer characteristics

* It can be noted that:
  - ↳ DAC O/p is result of multiplying the analog signal V_R by signal data. ∴ V_R is made variable, then DAC is called multiplying DAC [MDAC].
  - ↳ Higher the value of n, finer is the resolution of conversion, & closer is the staircase to a continous ramp waveform. DAC available for 6bit to 20bits.
  - ↳ Op-amp can be connected in non-inverting mode also.
  - ↳ Op-amp is operated as current to voltage convertor.
  - ↳ Polarity of V_R is chosen depending on switches to be operated
  - ↳ Accuracy & stability of DAC based on accuracy of resistors & their temperature depedance & also to handle varying current based on bit values.

When i/p is MSB LSB
001

$b_1 = 0$, $b_2 = 0$; $b_3 = 1$

$$V_0 = k V_{FS} \left[b_1 2^{-1} + b_2 2^{-2} + b_3 2^{-3} \right]$$

$$V_0 = 1 (V_{FS}) \left[0 (2^{-1}) + 0 (2^{-2}) + 1 (2^{-3}) \right]$$

Assume $k = 1$ & $V_{FS} = 8V = V_R$

$$V_0 = V_R \left[2^{-3} \right]$$

$$V_0 = \frac{V_R}{2^3} = \frac{V_R}{8}$$

$$V_0 = \frac{8}{8} = 1V$$

Disadvantage:

↳ Requirement of wide range of resistor values.

↳ As the length of binary word is increased, the range of resistor values needed also increases.

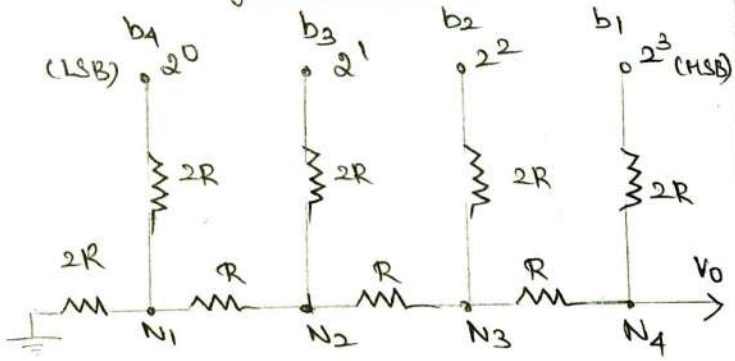
↳ Fabrication of such large value of resistors of order of MΩ is not practically possible.

↳ Voltage drop variation affects accuracy.

R-2R Ladder DAC

* A wide range of resistor value is required in the design of binary weighted resistor DAC.
* In R-2R ladder DAC resistors of only 2 values i.e, R & 2R are used. hence suitable for integrated circuit fabrication.
* Typical value of R vary from 2.5 KΩ to 10 KΩ.
* The principle of operation of a ladder type n/w for 4 bit DAC is shown with binary i/p b_1, b_2, b_3, b_4 & analog o/p V_0 & one terminating resistor.
* In this ladder circuit, the o/p voltage is a weighted sum of digital input.

Fig: 4bit R-2R ladder type DAC



For ex: 4 bit binary i/p

$b_1 b_2 b_3 b_4 = 1000$ i.e,

MSB = 1, Other i/p = 0.

Modified circuit is shown.

* The terminating resistor (2R) and resistor connected to b_4 i/p (2R) are combined at node N_1 to form an equivalent resistor R as shown in 1st stage.

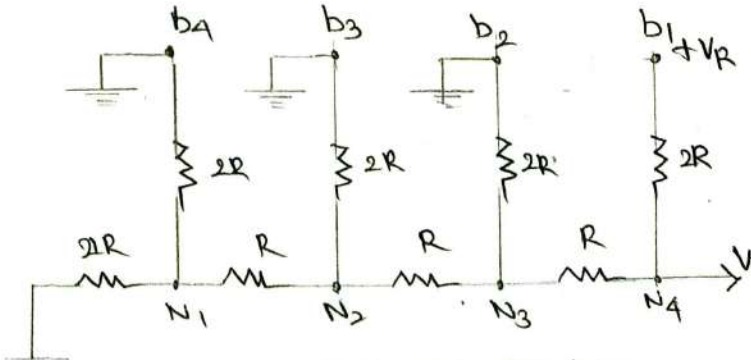


Fig: Equivalent ckt for binary i/p $b_1 b_2 b_3 b_4 = 1000$

* Then node N_2, the resistor connected with b_3 i/p (2R) can be combined with resistor (R+R = 2R) to form the 2nd stage of equivalent circuit is shown.

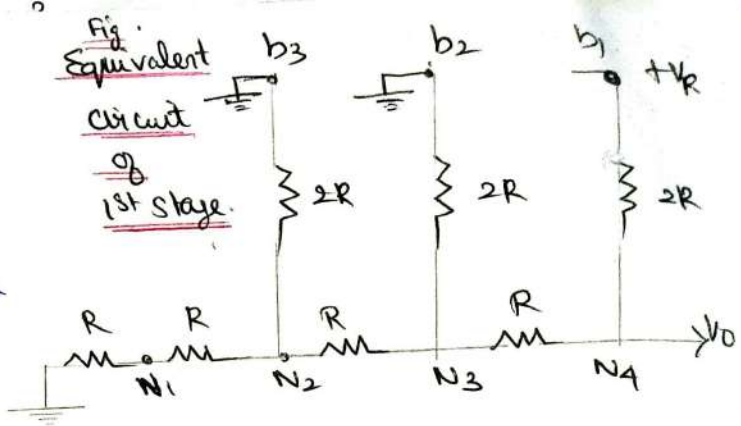


Fig: Equivalent circuit of 1st stage.

IIIly at N_3, the equivalent circuit of 3rd stage., where equivalent resistor R is obtained.

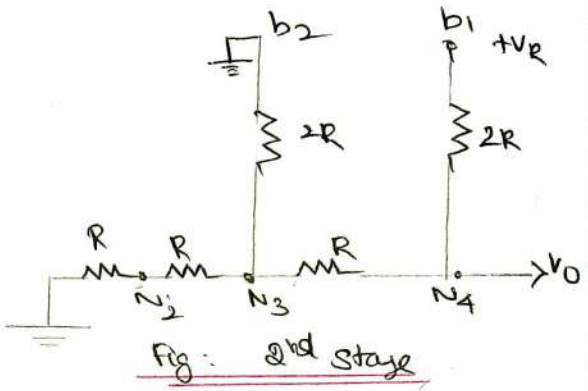


Fig: 2nd stage

Then, the analog o/p voltage V_0 is.

$$V_0 = \frac{V_R \times 2R}{R+R+2R} = \frac{V_R}{2} \quad -(4)$$

Thus for digital i/p $b_1 b_2 b_3 b_4 = 1000$

$V_0 = V_R/2$.

IIIly for $b_1 b_2 b_3 b_4 = 0100 \Rightarrow V_0 = V_R/4$

$b_1 b_2 b_3 b_4 = 0010 \Rightarrow V_0 = V_R/8$

$b_1 b_2 b_3 b_4 = 0001 \Rightarrow V_0 = V_R/16$

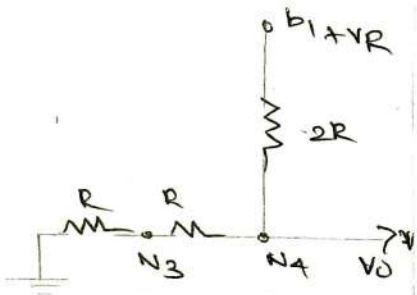


Fig: 3rd stage

Since the resistive ladder is a linear network, the principle of superposition can be used to find the total analog o/p voltage for a particular digital i/p by adding the o/p voltages caused by individual digital i/p's.

n-bit DAC is. $V_0 = \frac{V_R}{2^1} + \frac{V_R}{2^2} + \cdots \frac{V_R}{2^n} \quad -(5)$

n = total of bits at the i/p.

* The practical arrangement of 4 bit DAC using op-amp is shown.
* The inverting i/p terminal of the op amp act as summing junction for the ladder inputs.

Using eq (5) $V_0 = -V_R \frac{R_f}{R} \left(\frac{b_1}{2^1} + \frac{b_2}{2^2} + \frac{b_3}{2^3} + \frac{b_4}{2^4} \right) \quad -(6)$

$$V_0 = -V_R \frac{R_f}{R \times 2^4} [b_1 2^3 + b_2 2^2 + b_3 2^1 + b_4 2^0]$$

(ii) Generally for an n-bit i/p signal.

$$V_0 = \frac{-V_R}{2^n} (b_1 2^{n-1} + b_2 2^{n-2} + .. b_n 2^0)$$

The resolution of R/2R ladder type DAC, with current o/p is

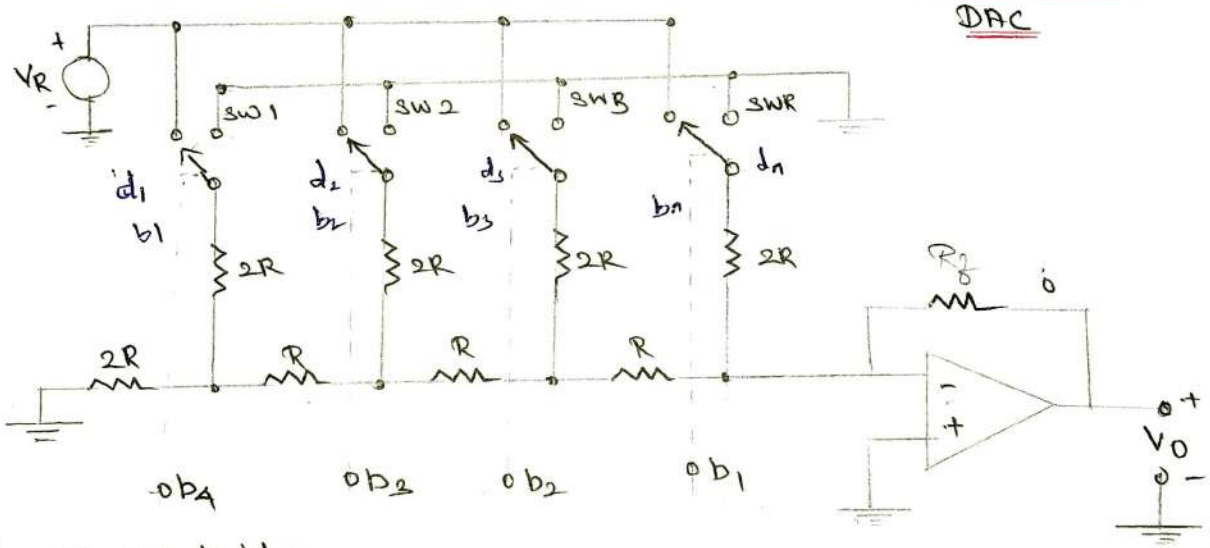
$$\text{Resolution} = I = \frac{1}{2^n} \times \frac{V_R}{R}$$

The resolution of the R/2R ladder type DAC with voltage i/p is

$$\text{Resolution } V = \frac{1}{2^n} \times \frac{V_R}{R} \times R_f.$$

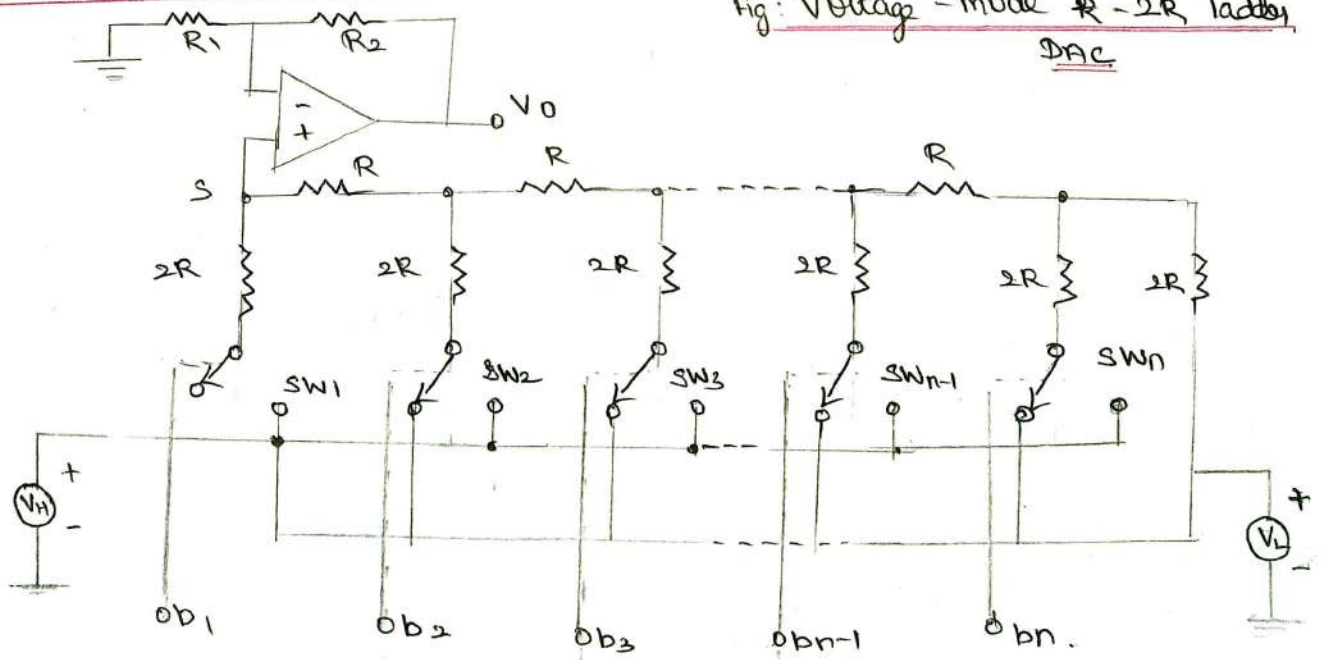
R_f = feedback resistance.

Fig: Four Bit R/2R Ladder DAC



Voltage Mode R-2R Ladder

Fig: Voltage-mode R-2R ladder DAC



* Shows the alternate circuit arrangement of the R-2R ladder type called voltage-mode R-2R ladder D/A Converter.
* The 2R resistors are switched between the two voltages level V_L and V_H as determined by the bit values $b_1, b_2 \cdots b_n$.
* The output from ladder is obtained at the left most ladder node s, buffered at the o/p of Op-amp.
* The two voltages V_L and V_H can be any 2 voltages levels.
* As the i/p binary word changes from 0...0 (all obits) to 1...1 (all 1 bits), the voltage of node s changes correspondingly in step of $2^{-n}(V_H - V_L)$ from the minimum voltage of $V_0 = V_L$ to the maximum of $V_0 = V_H - 2^{-n}(V_H - V_L)$.

Advantages of R-2R type DAC are:
(i) more accurate selection and design of resistor R and 2R are possible and
(ii) the binary word length can be increased by adding required number of R-2R sections.

Inverted or Current-mode R-2R Ladder DAC

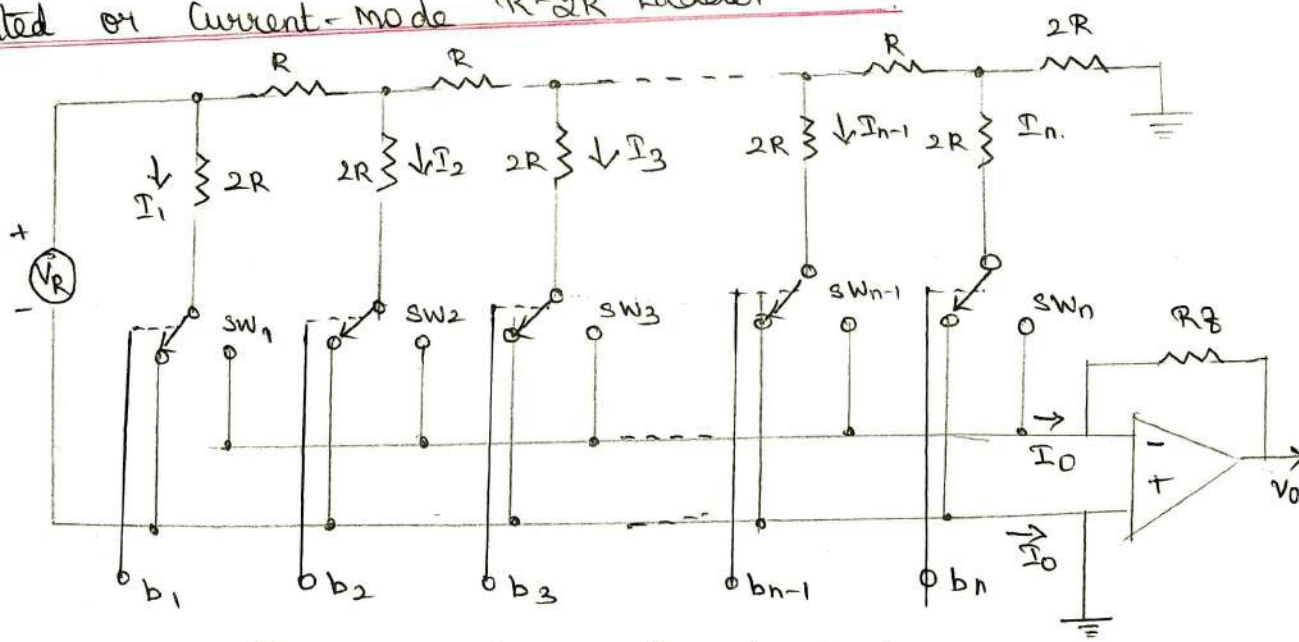


Fig: Inverted or Current-mode R-2R Ladder DAC

* In weighted resistor and R-2R ladder type of DAC the current flowing through the resistors changes as the input data changes.

* Power dissipation causes heating, and non-linearity of D/A conversion occurs due to varying power dissipation values corresponding to bit patterns.
* This becomes a serious limitations as the word length increases. This is eliminated in the inverted R-2R ladder type of D/A converter.
* The bit position of each of the subsequent MSBs and LSBs are interchanged.
* Each binary i/p is connected through the switch to either ground or to inverting i/p terminal of op amp, which is at virtual ground.
* Since both the positions of switch bi are at ground potential i.e, the actual or virtual ground, the current flow through any resistor is constant and it is independent of the i/p binary bit value.

These currents can be represented as.

$$I_1 = \frac{V_R}{2R} \quad -(7)$$

$$I_2 = \frac{(V_R/2)}{2R} = \frac{V_R}{4R} = I_1/2 \quad -(8)$$

$$I_3 = \frac{(V_R/4)}{2R} = \frac{V_R}{8R} = \frac{I_1}{4} \quad -(9)$$

$$I_n = \frac{(V_R/2^{n-1})}{2R} = \frac{I_1}{2^{n-1}} \quad -(10)$$

Output voltage V_0 is

$$V_0 = -I_0 \times R_f.$$

$$= -R_f (I_1 + I_2 + I_3 + \cdots + I_n)$$

$$= -\frac{V_R R_f}{R} (b_1 2^{-1} + b_2 2^{-2} + \cdots + b_n 2^{-n})$$

When $R_f = R$; $V_0 = -V_R (b_1 2^{-1} + b_2 2^{-2} + \cdots + b_n 2^{-n})$

* The circuit operation on the principle of summation of the currents. Hence it is called R-2R ladder current mode type of DAC.

* The current divides equally in successive nodes. & current flow in individual arms of the network remains the same irrespective of binary bit pattern.

∴ currents are maintained constant in all the branches and the ladder node voltages also remain constant at $V_R/2^0$, $V_R/2$, $V_R/2^2$ ... $V_R/2^{n-1}$.

* Op-amp is used as a I-V converter & total current I_o is determined by binary word.

Advantage:

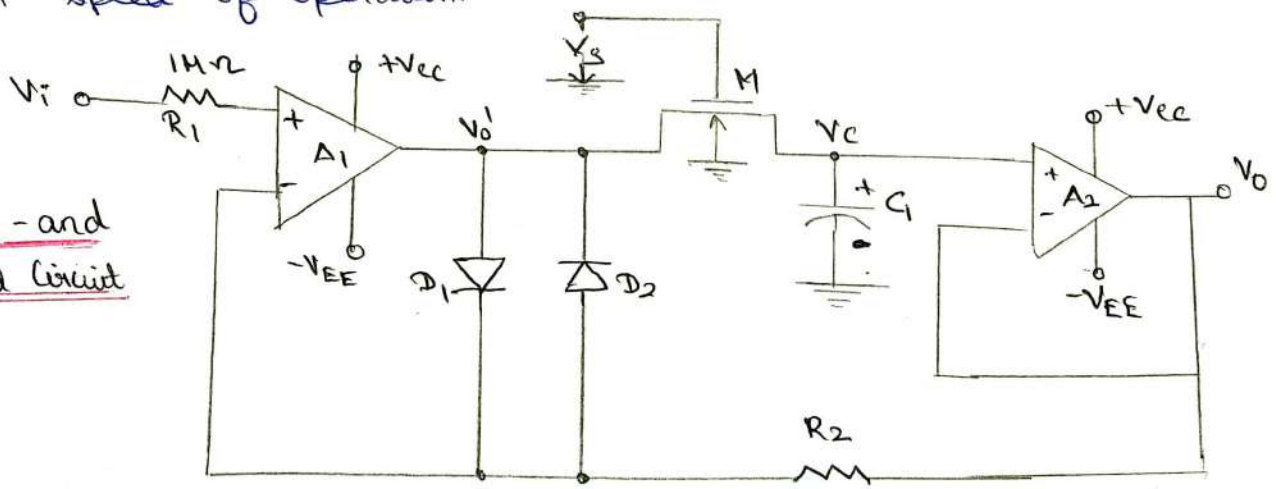
→ Stray capacitances do not affect the speed of response of the circuit due to the constant ladder node voltages.

→ Hence speed performance is improved.

→ Capability of using any 2 voltage level for the bit switching, neither of which needs necessarily be zero.

High Speed Sample and Hold Circuit

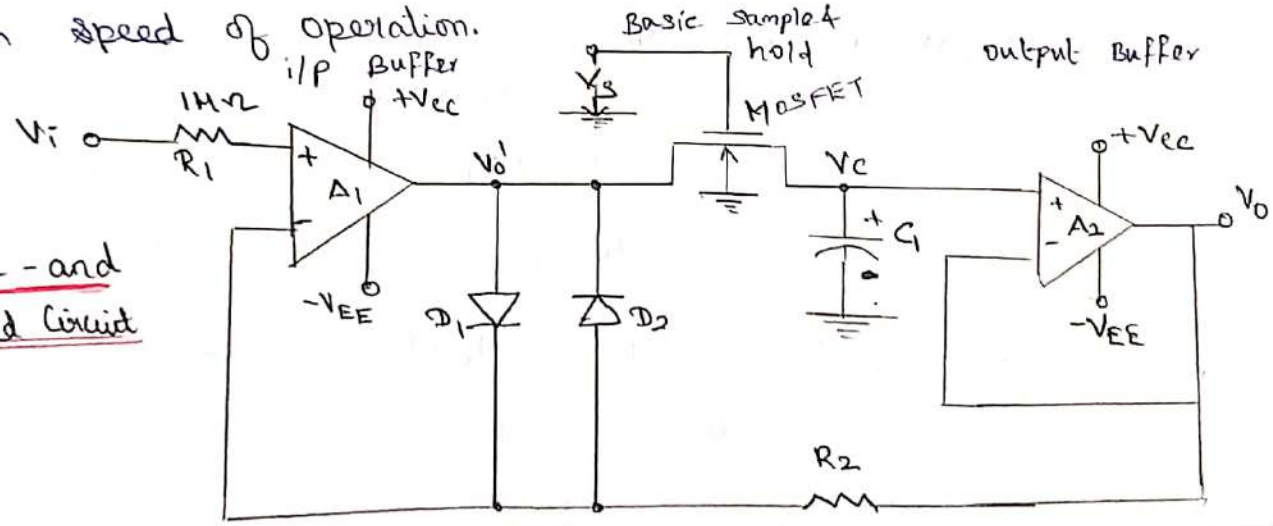
* The basic principle of sample and hold circuit is dealt with is shown below fig, shows a sample and hold circuit for high speed of operation.



Sample-and Hold Circuit

High Speed Sample and Hold Circuit

* The basic principle of sample and hold circuit is dealt with is shown below fig, shows a sample and hold circuit for high speed of operation.



Sample - and Hold Circuit

changes.

* The MOS transistor M shown is an analog switch capable of switching by logic levels, such as that from TTL.
* It alternately connects and disconnects the capacitor C_1 to the o/p of op-amp A_1.
* Diode D_1 & D_2 are inverse-parallel connected. They prevent op-amp A_1 from getting into saturation when the transistor M is OFF.
* This makes the operation of the circuit faster. Hence, the o/p of op.amp A_1 will be $V_o'(t) = V_i(t) - 0.7V$ when $V_i(t) < V_o(t)$ and $V_o'(t) \approx V_i(t) + 0.7V$ when $V_i(t) > V_o(t)$.
* when transistor M is ON, Op-amp A_1 & A_2 act as voltage follower
* The waveform is shown in below figure, it illustrate the Operation of the circuit.
* The transistor M is alternately switched ON and OFF by the control voltage V_s at the gate terminal.
* Note that the voltage V_s is to be higher than the threshold voltage of FET.
* when the transistor switch M is ON for a short interval of time, the capacitor C_1 quickly charges or discharges to the value of the analog signal at that instant.
* when input V_i is larger than capacitor voltage V_c and the transistor M is OFF, it rapidly charges to the level of V_i the instant M switches ON.
  Similarly if V_c is initially greater than V_i then C_1 rapidly discharges to the level of V_i when M becomes ON.
* when M is OFF, only the input bias current of opamp A_2 & the gate-source reverse leakage current of FET are effective in discharging the capacitor.

* Hence, the sampled voltage is held constant by C_1 until the next sampling instant or acquisition time.

* The below fig shows the sampling or acquisition time t_1 and holding time t_2.

* During the sampling time t_1, C_1 is charged through the FET channel resistance $R_{DS(ON)}$, and the charging time $t_1 = 5R_{DS(ON)}C_1$. When the capacitor charges to 0.993 of input voltage.

* During the hold time t_2, the capacitor partially discharges.

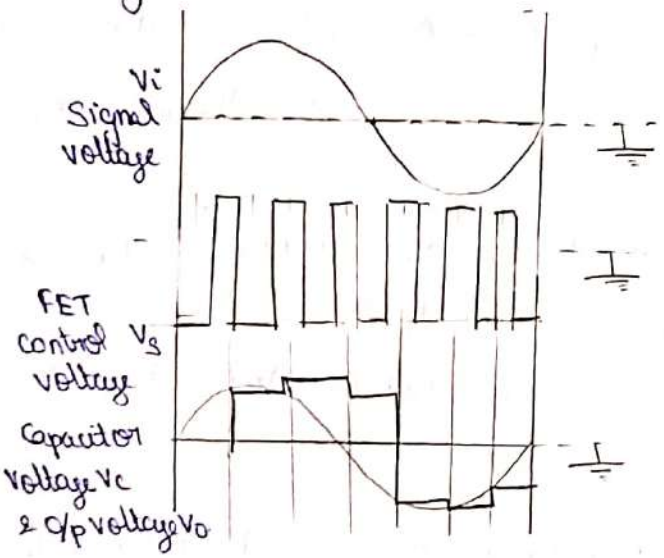


Fig: Signal voltage, control voltage & output voltage waveforms.

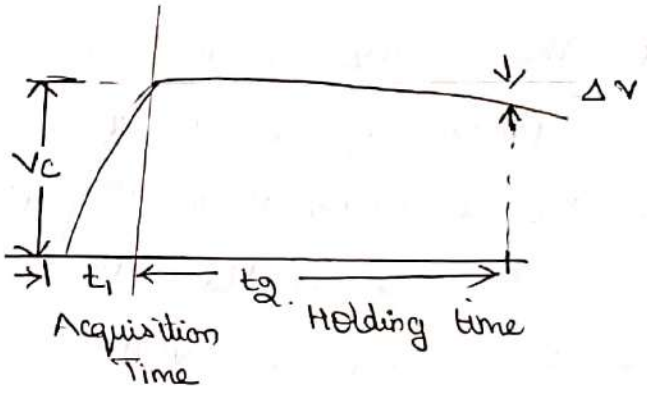
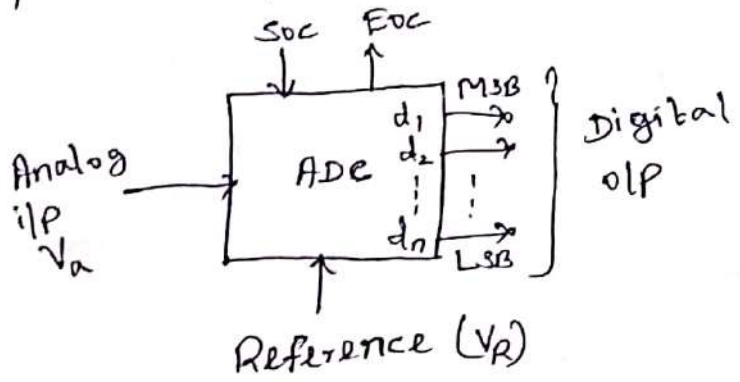


Fig: Capacitor voltage waveform

* This is called hold-mode droop. To avoid this, Op amp A_2 must have very low i/p bias current, the capacitor should have a low leakage dielectric and M must have very low reverse leakage current between its gate and source terminals.

* The low channel resistance $R_{DS(ON)}$ is desirable for the FET to achieve faster charging & discharging of C_1.

ANALOG TO DIGITAL CONVERTER : [A/D CONVERTER]



Schematic of ADC

The input is an analog signal and output is digital word.

The output digital word is generated with respect to reference voltage V_R and i/p s/l.

The functional value of D is.

$$D = d_1 2^{-1} + d_2 2^{-2} + d_3 2^{-3} + \dots + d_n 2^{-n}$$

$d_1 \rightarrow$ MSB & $d_n \rightarrow$ LSB

Types:

(i) Direct Type ADC [directly converts A to D]

(ii) Indirect type ADC. [Initially converts A to time & frequency and then converts to D]
(a) Integrating Type ADC

(i) Direct Type ADC

1. Flash Type [Comparator Type] Converter
2. Counter Type Converter
3. Tracking (or) servo converter
4. Successive Approximation type converter

(ii) Integrating Type ADC:

1. charge Balancing ADC
2. Dual slope ADC.

SIMULTANEOUS TYPE (FLASH TYPE) A/D CONVERTER

* The simultaneous type ADC is based on comparing an unknown analog i/p voltage with a set of reference voltages.
* To convert an analog signal into a digital signal of n output bits $(2^n - 1)$ number of comparators are required.
* For eg: 2 bit ADC requires 3 or $(2^2 - 1)$ comparator, while 3bit require 7 or $(2^3 - 1)$ comparators.
* Block Diagram of a 2 bit simultaneous type ADC is shown.

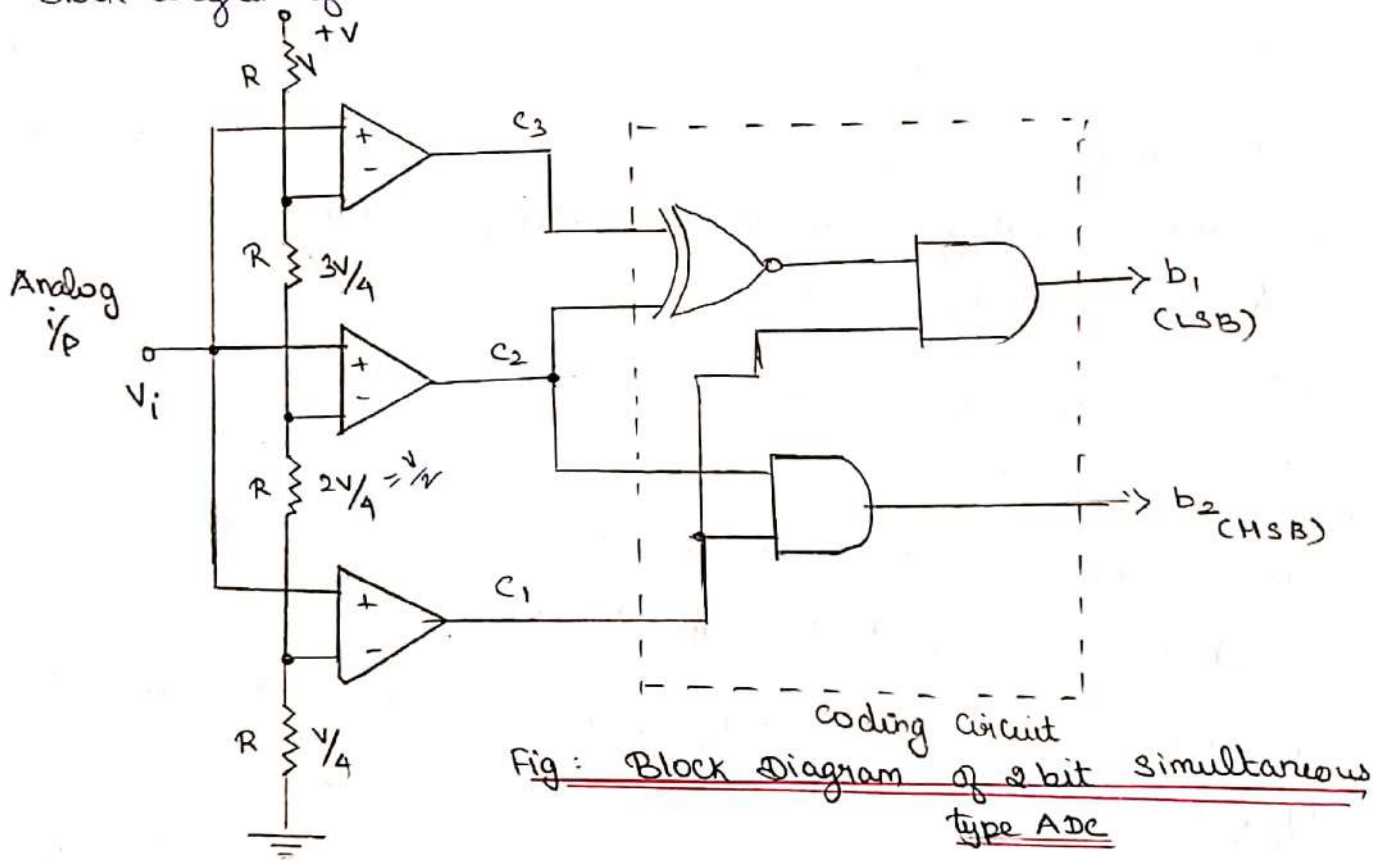


Fig: Block Diagram of 2 bit simultaneous type ADC

Table: Comparator & Digital o/p for a 2 bit simultaneous type ADC

Analog I/P voltage(V_i)	Comparator o/p			Digital o/p	
	C_1	C_2	C_3	b_2	b_1
$0 \le V_i \le V/4$	0	0	0	0	0
$V/4 \le V_i \le V/2$	1	0	0	0	1
$V/2 \le V_i \le 3V/4$	1	1	0	1	0
$3V/4 \le V_i \le V$	1	1	1	1	1

* As shown in fig, the 3 opamps are used as comparators.
* The non-inverting inputs of all the three comparators are connected to the analog input voltages.
* The inverting input terminal of the opamps are connected to a set of reference voltages $V/4$, $2V/4$ & $3V/4$ respectively, which are obtained using a resistive divider network & power supply $+V$
* The output of a comparator is in positive saturation state when the voltage at the non-inverting i/p terminals is more than the voltage at the inverting terminal and it is in negative saturation state otherwise
* When the analog i/p voltage is less than $V/4$, the voltage at the non-inverting terminals of the 3 comparators is less than their respective inverting input terminal voltages. & hence, the comparator o/p are $c_1 c_2 c_3 = 000$.
* When analog i/p is between $V/4$ & $V/2$, the comparator o/p's are $c_1 c_2 c_3 = 100$.
* Since there are 4 ranges of analog i/p voltages, this can be coded using 2 bit digital o/p $(b_2 b_1)$.
* The coding circuit for encoding the 3 comparator o/p into 2 digit o/p's is shown inside the dotted square. using the simplified expressions for b_1 & b_2.
* The logic expressions for b_2 & b_1 can be written as

$$b_2 = c_1 c_2 \bar{c_3} + c_1 c_2 c_3 = c_1 c_2 (\bar{c_3} + c_3) = c_1 c_2$$

$$b_1 = c_1 \overline{c_2 c_3} + c_1 c_2 c_3 = c_1 (c_2 \oplus c_3)$$

* n'ly, 3 bit ADC can be constructed using seven $(2^3 - 1)$ comparators
* The comparators & digital o/p for 8 different ranges of analog i/p voltage are given below.

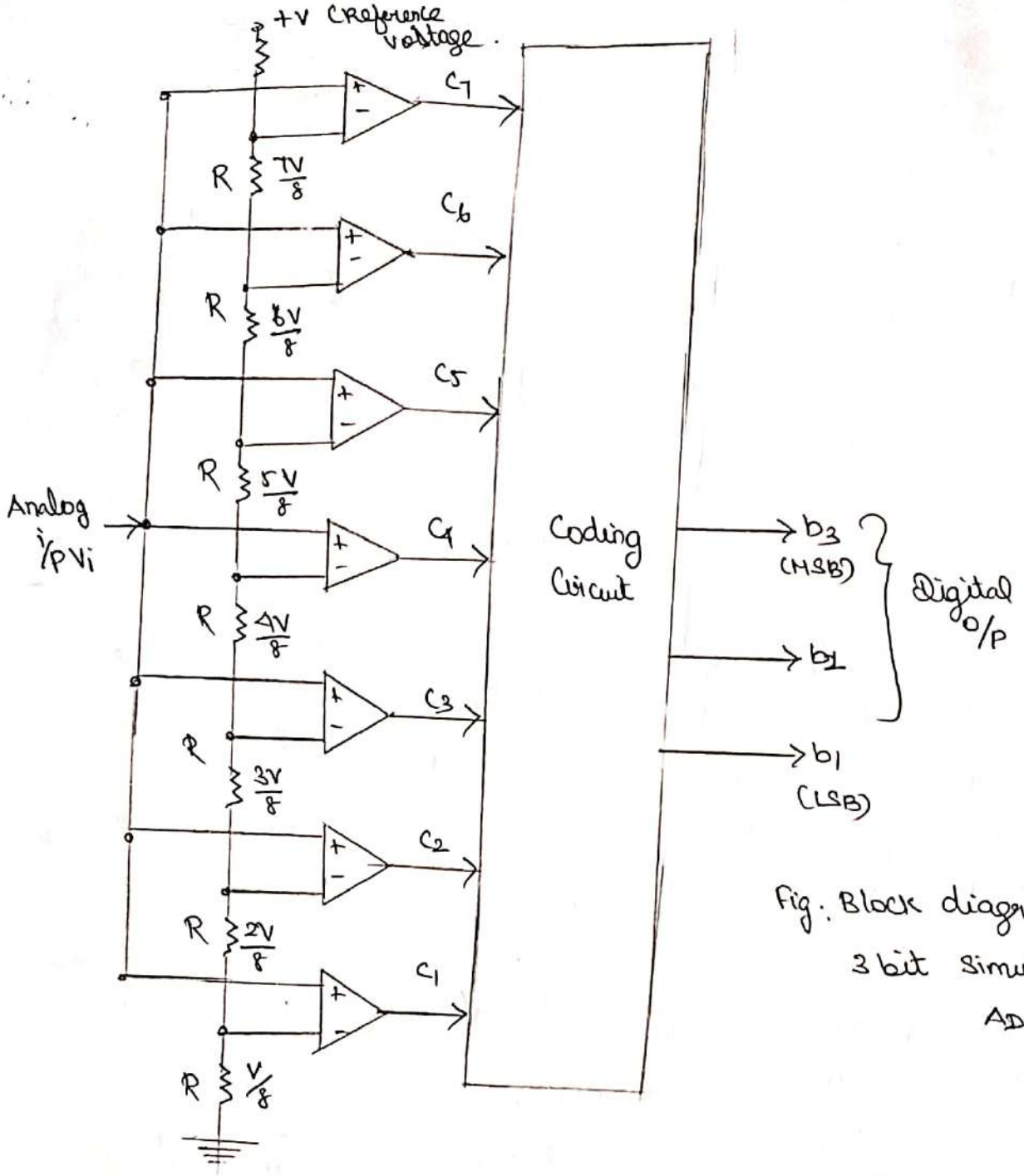


Fig: Block diagram of 3 bit simultaneous type ADC.

Analog Input voltage V_i	Comparator o/p							Digital o/p		
	C_1	C_2	C_3	C_4	C_5	C_6	C_7	b_3	b_2	b_1
$0 \le V_i \le V/8$	0	0	0	0	0	0	0	0	0	0
$V/8 \le V_i \le 2V/8$	1	0	0	0	0	0	0	0	0	1
$V/8 \le V_i \le 3V/8$	1	1	0	0	0	0	0	0	1	0
$V/8 \le V_i \le 4V/8$	1	1	1	0	0	0	0	0	1	1
$V/8 \le V_i \le 5V/8$	1	1	1	1	0	0	0	1	0	0
$V/8 \le V_i \le 6V/8$	1	1	1	1	1	0	0	1	0	1
$V/8 \le V_i \le 7V/8$	1	1	1	1	1	1	0	1	1	0
$V/8 \le V_i \le V$	1	1	1	1	1	1	1	1	1	1

* It is clear that the logic expression for (b_3, b_2, and b_1) are complex due to their dependence on seven input variables ($C_1, C_2 \ldots C_7$)

* Hence, the coding circuit is implemented using a priority encoder.

* IC74148 is an 8 to 3 priority encoder with active LOW i/p & o/p's

* Since the comparator o/p's are active HIGH, they are connected to the i/p's of encoder through inverters and the o/p's of encoder are inverted once again to get active HIGH digital o/p's b_3, b_2 and b_1.

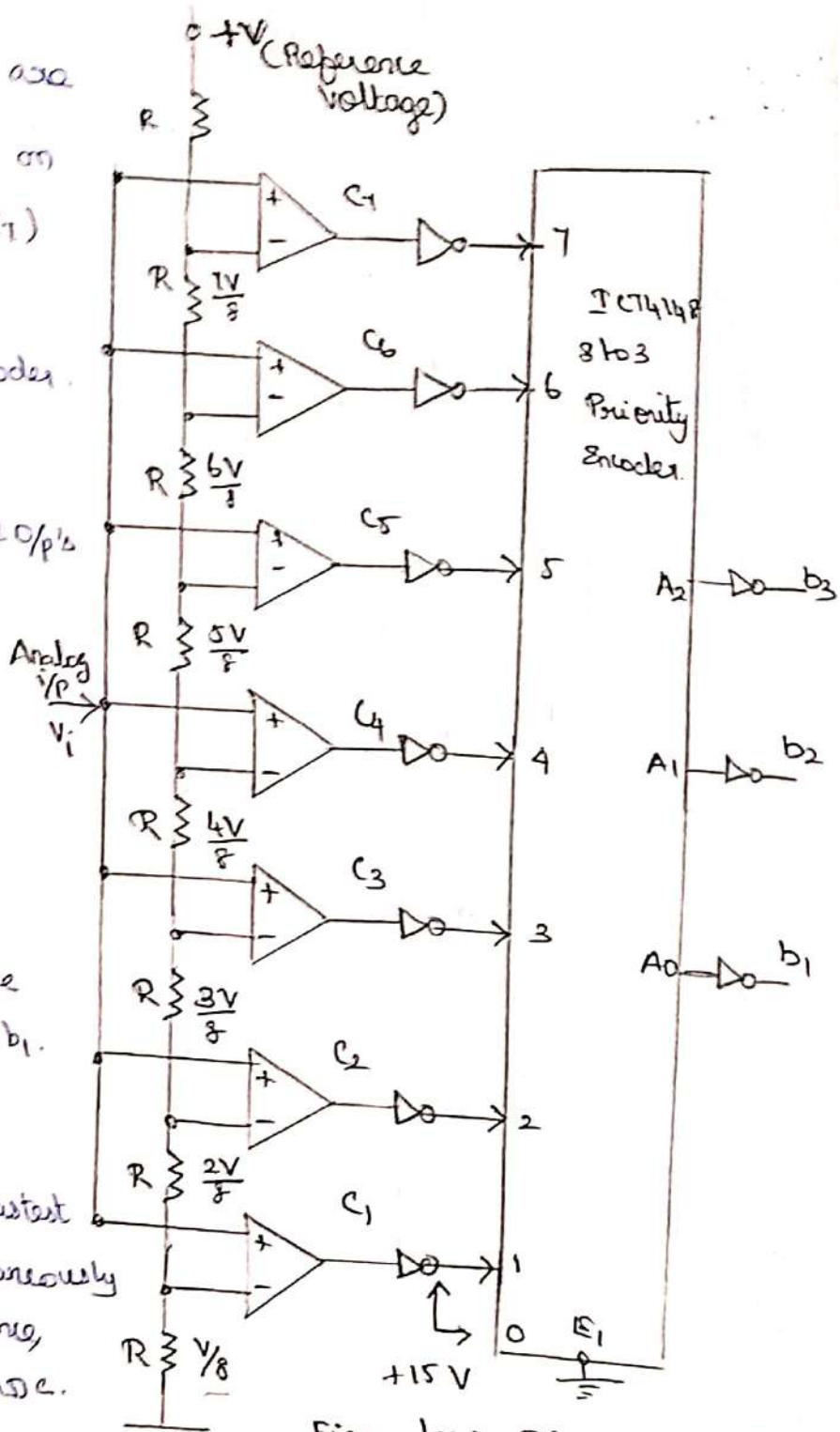


Fig: Logic Diagram of 3-bit Simultaneous type ADC

Advantages:

* Simultaneous type ADC is the fastest because ADC is performed simultaneously through a bat of comparators. Hence, it is also called flash type ADC. Typical conversion time is 100 n s orders

* Construction is simple and easier to design

Disadvantages:

* The simultaneous type ADC is not suitable for ADC with more than 8 or 4 digital o/p bits.

* Total $(2^n - 1)$ comparators are required for an n-bit ADC and number of comparators required doubles for each added bit.

Successive Approximation Type ADC

* Conversion time is maintained constant in an successive approximation type ADC and it is proportional to the number of bits in the digital O/P, unlike the counter and continuous type ADC.

* The basic principle of this ADC is that the unknown analog i/p voltage is approximated against an n-bit digital value by trying one bit at a time, beginning with the MSB.

* The principle of successive approximation process for a 4bit conversion is shown below.

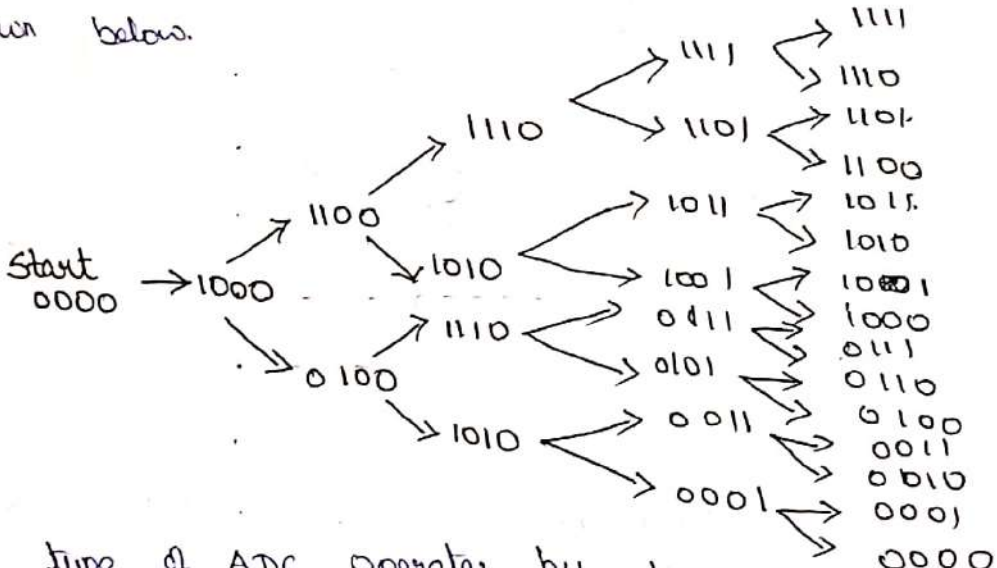


Fig: Principle of 4 bit digital O/P.

* This type of ADC operates by successively dividing the voltage range by half, as explained in the following steps.

↳ The MSB is initially set to 1 with remaining 3 bits set to 0. The digital equivalent is compared with the unknown analog i/p voltage

↳ If the analog i/p voltage is higher than the digital equivalent, the MSB is retained as 1 and the second MSB is set to 1. Otherwise, the MSB is reset to 0 and second MSB is set to 1.

↳ Comparison is made as given in step 1 to decide whether to retain or reset the 2nd MSB. The 3rd MSB is set to 1 and the operation is repeated down to LSB and by this time, the converted digital value is available in the SAR.

* From above figure., it can be seen that the conversion time is constant (i.e 4 cycle for 4 bit ADC) for various digital O/P's

* This method uses a very efficient search strategy to complete an n-bit conversion in just n-clock periods.
* ∴ for an 8 bit successive approximation type ADC, the conversion requires only 8 cycles, irrespective of the amplitude of analog i/p voltage.
* The functional block diagram of successive approximation type ADC is shown below.

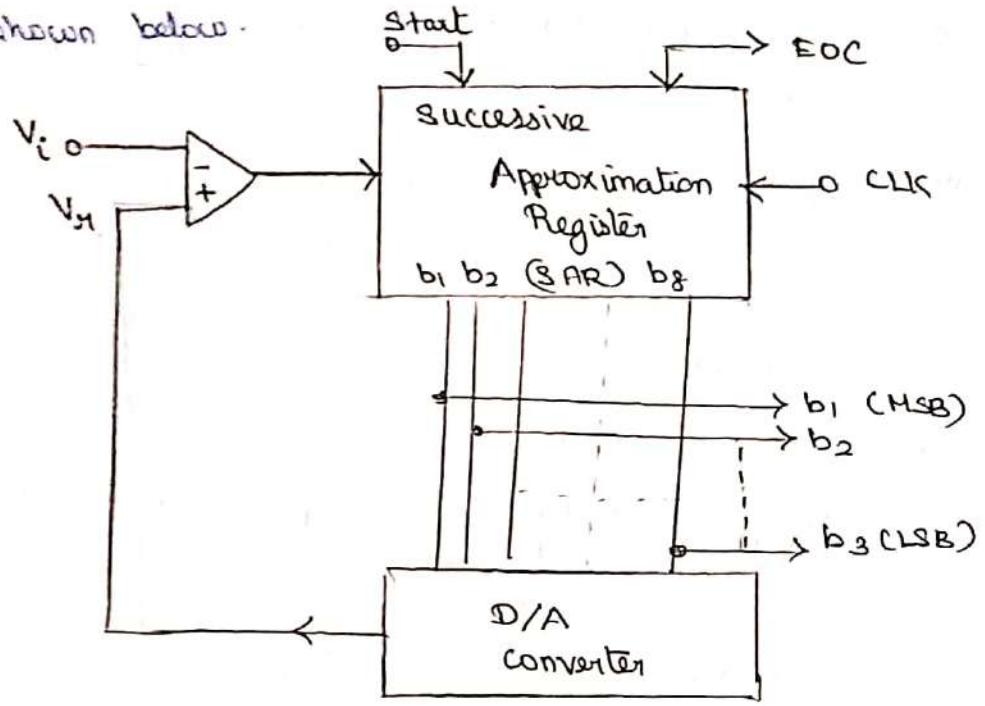


Fig: Functional Block Diagram of Successive Approximation Type ADC

* The circuit employs a successive approximation register (SAR) which finds the required value of each successive bit by trial & error method.
* The o/p of SAR is fed to an n-bit DAC.
* The analog o/p equivalent to digital to analog converter is applied to the non-inverting i/p of the comparator, while the other i/p of the comparator is connected with an unknown analog i/p voltage V_i under conversion.
* The comparator o/p is used to activate the successive approximation logic of SAR.
* When the START command is applied, SAR sets the MSB (b_1) of the digital signal, while the other bit made zero, so that the trial code becomes 10000000.
* The o/p of SAR is converted into analog equivalent V_f and gets compared with the i/p signal V_i.

* If V_i is greater than DAC o/p, then the trial code is less than the correct digital value.
* The MSB is retained as 1 and the next significant bit is made 1 and the testing is repeated.
* If the analog i/p V_i is now less than DAC o/p, then the value 11000000 is greater than the exact digital equivalent.
* Therefore, the comparator reset the second MSB to 0 and proceeds to the next most significant bit.
* This process is repeated for all the remaining lower bits in sequence until all the bit position are tested.
* The EOC signal is sent out when all the bits are scanned and the value of DAC o/p just crosses V_i
* Table below shows the flow of conversion sequence and fig shows the o/p response with the associated waveforms.

Correct Digital Representation	Successive Approximation Register (SAR) o/p V_i at different stages in the conversion	Comparator o/p.
11010100	1000 0000	1 (Initial o/p)
	1100 0000	1
	1110 0000	0
	1101 0000	1
	1101 1000	0
	1101 0100	1
	1101 0110	0
	1101 0101	0
	1101 0100	

* It can be observed that the DAC o/p voltage gets successively closer to the analog i/p voltage V_i.
* For 8-bit ADC, it requires 8 pulses to compute the o/p irrespective of the value of the analog i/p
* AD7582 → 12 bit ADC → successive approximation technique used a 28-pin DIP CMOS package.

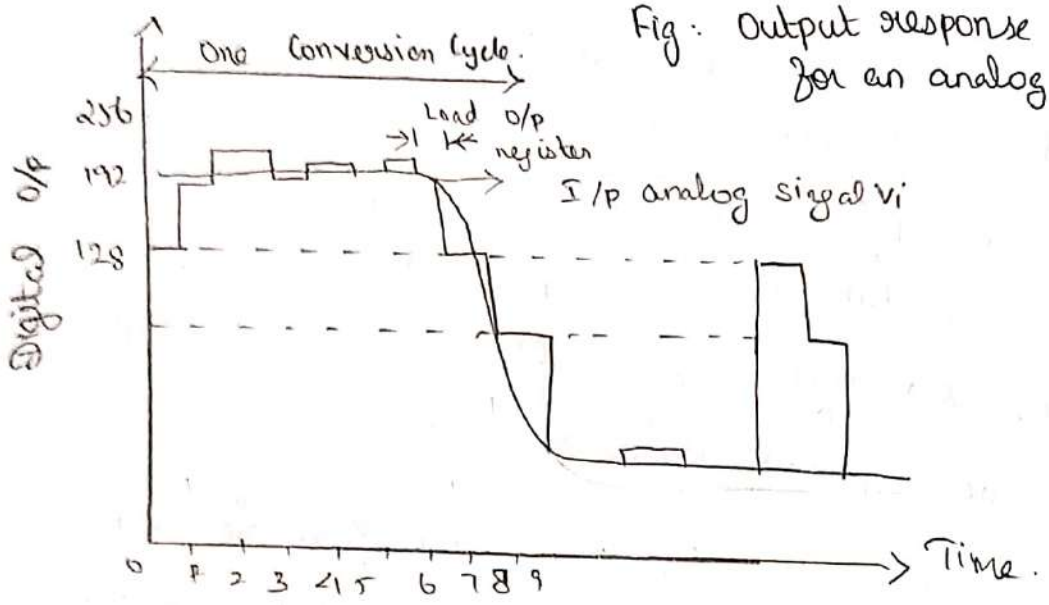
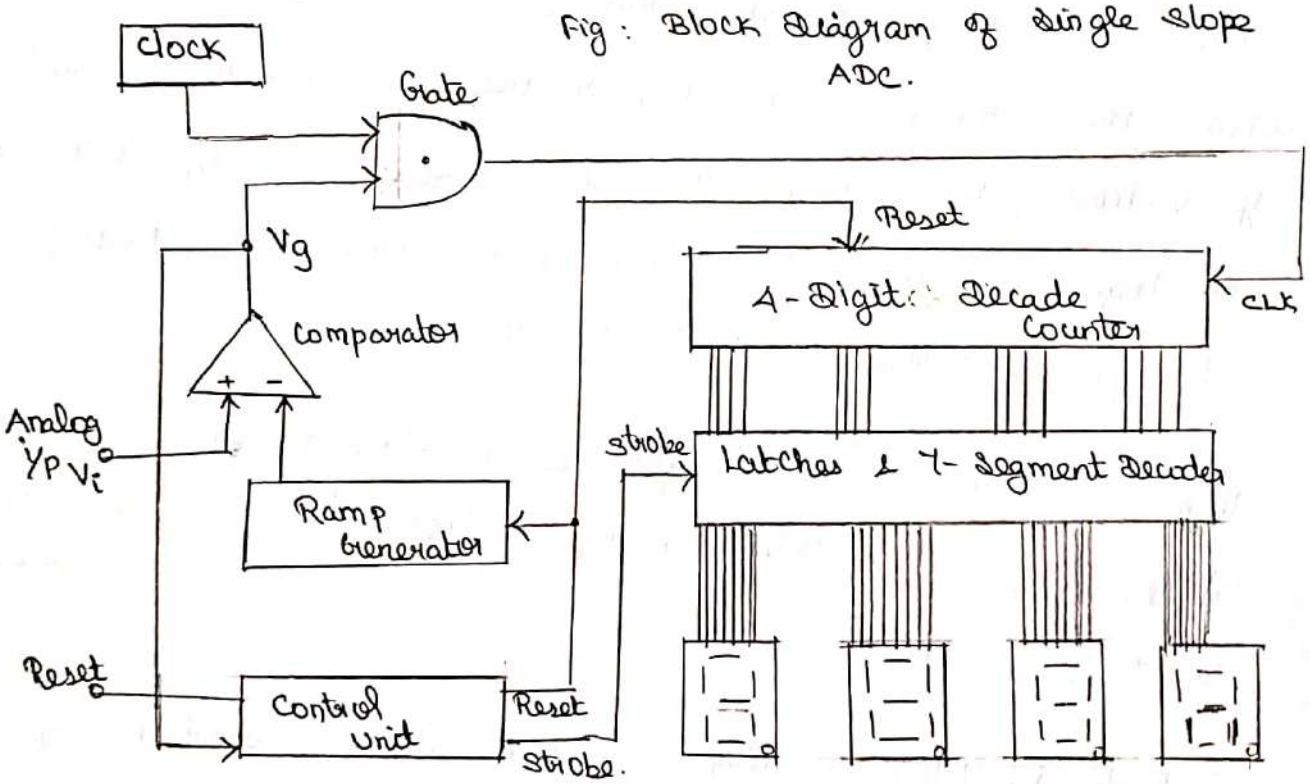


Fig: Output response for an analog i/p.

Single Slope Type ADC

* If short conversion time is not important, one can consider single or dual slope type A/D converter.
* These converter techniques are based on comparing the unknown analog i/p voltage with a reference voltage that begins at 0V & increases linearly with time.
* The time required for the reference voltage to reach the value of unknown analog i/p voltage is proportional to the amplitude of unknown analog i/p voltage.
* This time period can be measured using digital counter.
* The block diagram of single slope type ADC is shown.

Fig: Block Diagram of single slope ADC.



* The main circuit of this converter is a ramp generator, which on receiving a RESET from the control circuit increases linearly with time from 0V to a maximum voltage V_m.
* For Eg: if $V_m = 10V$ and it takes 1ms to move from 0V to 10V, then the slope is 10V/ms.
* Such a ramp generator can be either an opamp based integrator circuit or DAC driven by a sequence binary counter, whose o/p waveform

is a staircase increasing linearly. The operation of this converter is explained

* Assume that a positive analog i/p voltage V_i is applied at the non-inverting input of the comparator.
* Now, when a RESET signal is applied to the control logic, the 4 digit decade counter reset to 0
* and the ramp voltage begins to increase.
* Since V_i is positive, the comparator o/p is in HIGH state.
* This allows the CLK pulse to pass to the i/p of the 4 digit counter through the AND gate and the counter is incremented.
* This process continues, until the analog i/p voltage is greater than the ramp generator voltage.
* When the ramp generator voltage is equal to the analog i/p voltage, the comparator o/p becomes negatively saturated or logic 0 and the clock is prevented from passing through the gate, casing the counter operation.
* Then the control circuit generates a STROBE signal, which latches the counter value in the 4 digit latch, which is displayed on 7-segment displays.
* The displayed value is then equivalent to the amplitude of analog i/p voltage.

For Eg. Clock value CLK = 1MHz, Slope of the ramp generator is 1V/ms, 4 digit decade counter reaches its full scale value is 9999 in 9999 μs ⇒ 9.999 ms, ramp generator voltage reaches 9.999V.

* So this single slope type ADC can display any analog i/p value from 0V to 9.999V.

* If V_i = 5.62V, counter require 5620 clock pulse to advance from 0000 to 5620., ramp voltage raise to 5.62V.
  ∴ Display 5620. ⇒ 5.620V.

Disadvantage:

→ Due to component value error and clock errors.

→ Integrated o/p voltage is a function of the product of R & C.
∴ Changes in the value of capacitance & Resistance due to temperature affect the integrated o/p & introduce error.

→ Drift in clock frequency cause error.

Dual slope Type ADC

* In dual slope type ADC, the integrator generates two different ramps, one with the unknown analog i/p voltage V_i as the i/p and another with a known refrence voltage $-V_R$ as the i/p.
* Hence it is called dual slope type ADC.
* The operation of dual slope type ADC is explained as follows.
* Assume that the 4-digit decade counter is initially reset to 0000, the ramp o/p V_s is reset to 0V, analog i/p voltage is positive, and the i/p to the ramp generator or integrator is switched to the unknown analog i/p voltage.
* Since the positive analog i/p voltage is connected to the inverting i/p of the integrator, the integrator o/p V_s is a negative ramp while the comparator o/p V_g is positive, and CLK passed through the AND gate

* This results in counting-up of the 4-diget decade counter.
* The negative ramp will proceed for a fixed time period T_1, which is determined by a count detector for the time period T_1.
* At the end of fixed time period T_1, the ramp voltage is given by

$$-V_s = \frac{V_i}{RC} \times T_1$$

RC = Time constant of the ramp generation circuit.

*

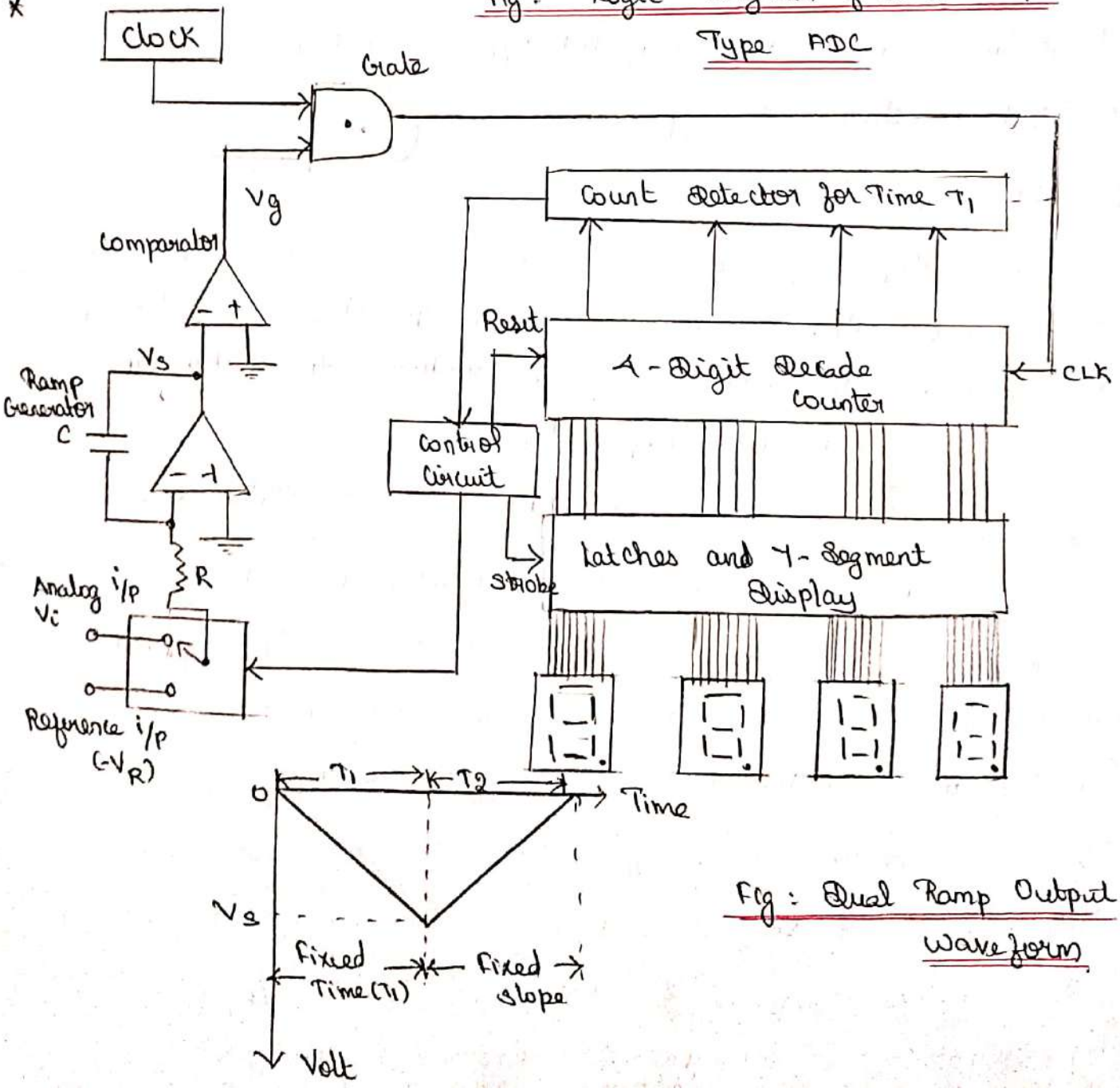


Fig: Logic Diagram of Dual Slope Type ADC

Fig: Dual Ramp Output Waveform

* when the counter reaches the fixed count at time period T_1, the count detector gives a signal to the control circuit which in turn resets the counter to 0 and switches the integrator i/p to a negative reference voltage ($-V_R$).

* Now, the ramp generator begins at $-V_s$ and increase upward until it reaches 0V.

* During this time, the counter gets advanced

* When V_s reaches 0V, the comparator o/p will become 0 and the CLK is inhibited from passing through the AND gate.

* Now, the conversion cycle is said to be completed and the positive ramp voltage is given by

$$V_s = -\left(\frac{-V_R}{RC} \times T_2\right)$$

V_R & RC are constant & time period T_2 is variable.

* Since the ramp generator voltage starts at 0V, decreasing down to $-V_s$ and then increasing up to 0V, the amplitude of negative and positive ramp voltages can be equated as follows,

$$-\frac{V_i}{RC} \times T_1 = \frac{V_R}{RC} \times T_2$$

$$-V_i = V_R \times \frac{T_2}{T_1}$$

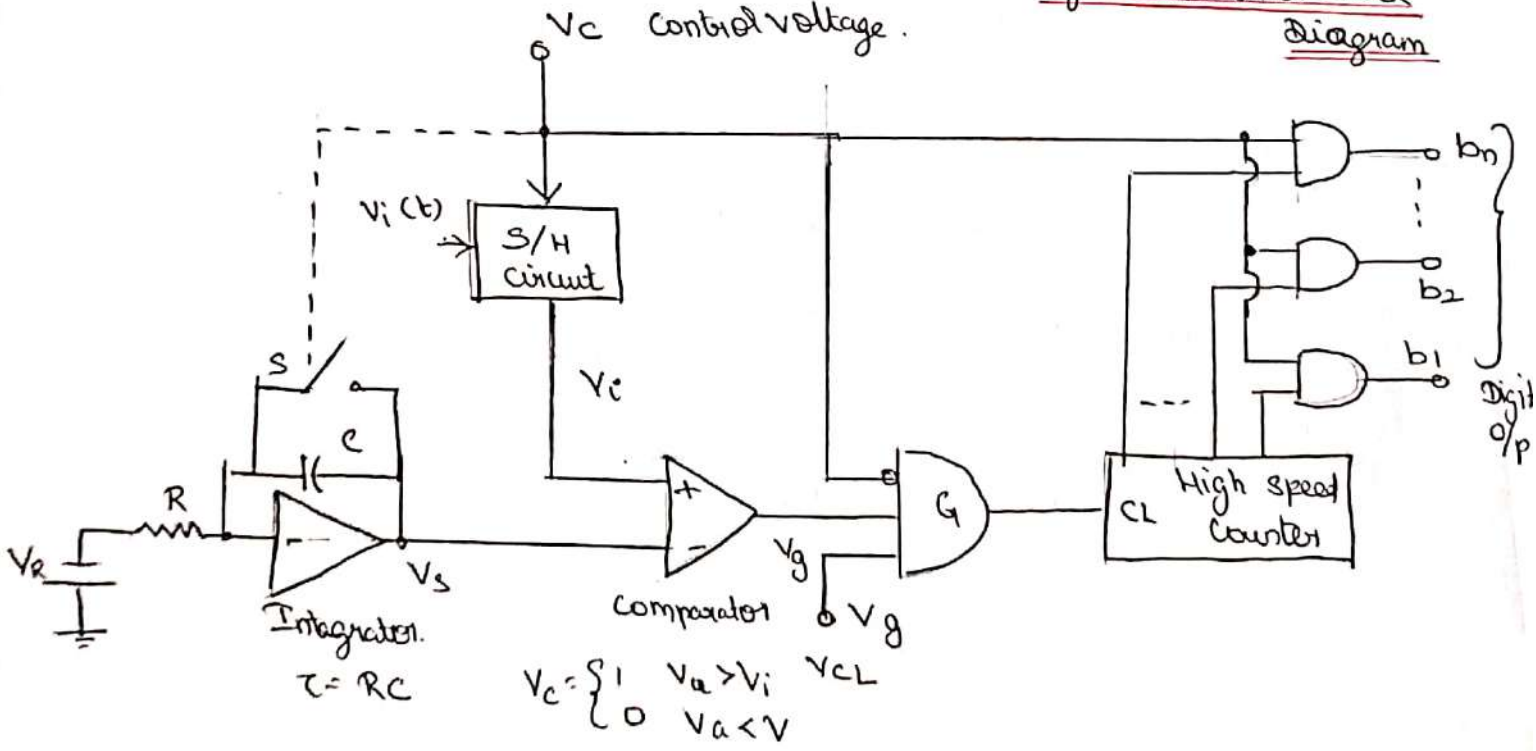
* From the above equation, it is clear that the unknown analog i/p voltage is proportional to the time period T_2, because V_R is known reference voltage. and T_1 is the predetermined time period.

* Also the contents of the 4-digit decade counter at the end of conversion reflect the variable time period T_2.

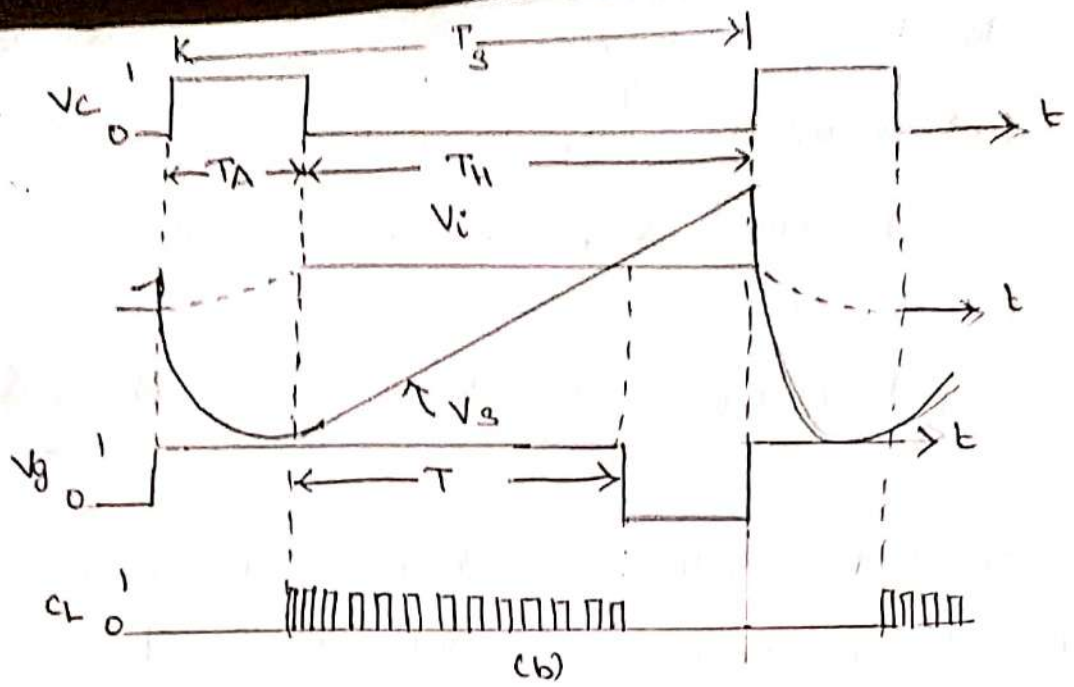
ANALOG TO DIGITAL CONVERTER USING VOLTAGE TO TIME CONVERSION

* An analog signal can be converted into digital signal by counting the pulses from a variable frequency source whose frequency is dependent on the analog i/p signal value.
* The counting is done for a fixed period of time.
* Alternatively, the pulses from a fixed frequency source can be counted for a variable period of time, and the time period is then dependent on the analog signal under conversion.

Fig. Functional Block Diagram



* The above figure shows such an ADC. It employs an integrator, a sample & Hold (S/H) circuit, a voltage comparator and high speed counter.
* A negative reference voltage V_R is applied to the integrator, which integrates the voltage V_R and provides a positive polarity o/p.



(b)

Fig: Input & output waveform

* The analog signal i/p under conversion $V_i(t)$ is sampled at a rate fixed by the control voltage V_C, and the sampled signal at any instant V_i is applied as i/p to the non-inverting terminal of comparator.
* The integrator o/p V_S is connected to the inverting i/p of comparator.
* When the integrated voltage V_S is less than the analog voltage sample V_i as shown., the comparator o/p is at positive saturation or at logic 1. $(V_S < V_i)$ = V_{sat} or 1
* A fixed frequency clock V_{CL} is applied to the high speed counter through the AND Gate G.
* The AND gate is enabled for the duration from $t=0$ when $V_i = 0$ to the time $t=T$ when $V_S = V_i$
* W.K.T $V_S = \frac{V_R t}{\tau}$ where time constant is given by $\tau = RC$ for integrator.

∴ at time $t=T$ when $V_S = V_i$, we can infer

$$T = \frac{\tau V_i}{V_R}$$

Assuming F_C is the clock frequency, the count o/p N obtained during the time interval 0 to T is given by

$$N = F_c T = \frac{T F_c V_i}{V_R}$$

Hence, the count value N is proportional to V_i

* The sample & Hold circuit samples the +ve i/p voltage $V_i(t)$ for every T_A.
* Then the sampled voltage V_i is held for a time duration indicated by T_H.
* During the period T_H, switch S is held open, and the integrator operates with its o/p following a ramp voltage waveform V_s.
* when $V_s < V_i$, the comparator o/p $V_y = 1$. Gate G_1 is enabled, with V_c = 0 state.
* This continues for a time interval T and during this time, the clock pulse are passed by the gate G_1 to the high speed counter.
* Thus the digital o/p of the counter is directly proportional to T.
* During this time interval T_A, the gate is disabled, and the digital o/p is read from the counter.
* The switch S is closed during T_A, the capacitor discharges, resetting V_s to 0V thus starting a new conversion.

Oversampling A/D converter

* Analog circuitry forms the most important part of a data converter.
* The resolution and speed of the data conversion are limited by the component mismatch and non-linearity of the components, drift ageing, noise, dynamic limitation and parasitic.
* Hence, over-sampling converters employing more complex digital circuitries are used.
* They sample the analog signal at a rate much higher than the sampling rate normally required with Nyquist converters.

DELTA MODULATION (DM)

* DM developed in 1940's is a differential pulse-code modulation (DPCM) technique, in which the derivation of the signal is quantized.
* When signal variations between the subsequent samples periods are very small, the word length of the quantizer can be reduced.
* With very high over-sampling rate, the changes between sample periods are made very small, and the quantizer can be reduced to low-bit.
* A 1 bit DPCM coder is known as a delta modulator (DM).
* DM codes the difference in the signal amplitude instead of the signal amplitude itself.
* The delta modulator A/D converter has the following processes:
  - The analog signal is approximated with a series of segments.

↳ Each segment of the approximated signal is compared with the original analog wave to determine the increase or decrease in relative amplitude.

↳ The decision procers of establishing the state of successive bit is determined by this comparison.

↳ Only the state related to change of information is sent, and a no-change condition causes the modulated signal to remain at the same 0 or 1 state of the previous sample.

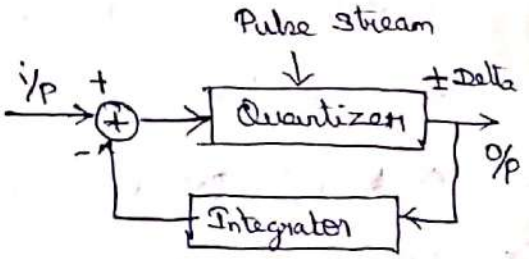
↳ Examples of delta Modulation technique are.
- → Continuously variable slope delta modulation.
- → Sigmal delta Modulation and
- → Differential Modulation.

* Delta modulation (DH) may be viewed as a simplified form of DPCH in which a 2 level (1 bit) quantizer is used in conjuction with a fixed first-order predictor.

* A DH encoder is shown below. It is known as a single integration modulator.

* The i/p signal is compared with the integrated o/p pulses and the delta (difference) signal is applied to the quantizer.

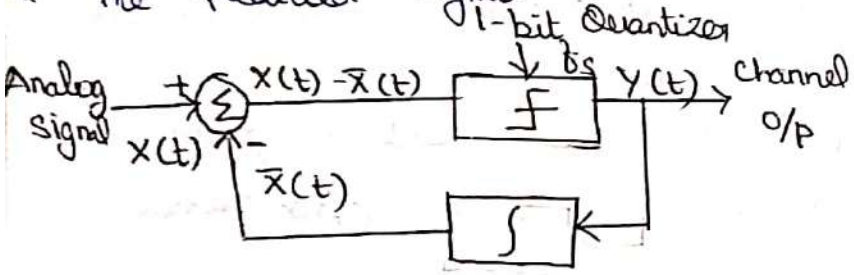
* The quantizer generates a positive pulse when the difference signal is negative and it generate a negative pulse when the difference signal is positive.



Delta Modulation Encoder.

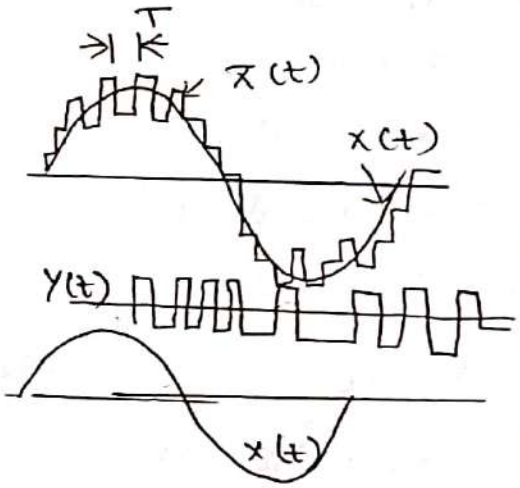
* The positive signal moves the integrator step by step closer to the present value of i/p, tracking the derivative of the i/p signal.

* The DM is based on quantizing the change in the signal from sample to sample rather than the absolute value of the signal at each sample.
* Since the o/p of the integrator in the feedback loop of figure tries to predict the i/p $x(t)$, the integrator works as a predictor.
* The prediction error term $x(t) - \bar{x}(t)$ in the current prediction is quantized and it is used to make the next prediction.
* The quantized prediction error which is the delta modulation o/p is integrated in the receiver just as it is in the feedback loop.
* i, the receiver predicts the i/p signals as shown.
* The predicted signal is smoothed with a low pass filter.



(a) Modulation.

(b) Demodulation.



* The delta modulators exhibit slope overload for rapidly raising i/p signals, and their performance is thus dependent on the frequency of the i/p signal.
* In theory, the spectrum of quantization noise of the prediction error is flat and the noise level is set by the 1-bit comparator.

Slope Overload Distortion:

The slope overload distortion is introduced due to the use of a step size delta that is too small to follow some portions of the waveform with a steep slope. It can be reduced by increasing the step size.

anular Noise :

The Granular noise results from using a step size that is too large in parts of the waveforms having a small slope. The granular noise can be reduced by decreasing the step size.

* An alternative solution is to employ a variable step size that adapts itself to the short-term characteristics of the source signal. Here, the step size is increased relatively small slope. This strategy is called Adaptive Delta Modulation (ADM).

Sigma-Delta (Σ-Δ) Modulator.

* DM requires two integrator for modulation and demodulation process as shown.
* Since integration is a linear operation, the second integrator can be moved ~~from~~ before the modulator without altering the overall i/p-o/p characteristics.
* Furthermore, the 2 integrators in fig, can be combined into a single integrator by the linear operation properly as shown.
* The arrangement shown is called a Sigma-Delta (Σ-Δ) modulator and its S-domain equivalent.
* This structure can be considered as being a smoothed version of a 1-bit delta modulator.
* The name sigma-delta modulator comes from the principle of placing the integrator (sigma) before the delta modulator.
* Sometimes, the (Σ-Δ) modulator is referred to as an interpolative coder.
* The quantization noise characteristic or the noise performance of such a coder is frequency dependent in contrast to the delta modulation.

LIC - UNIT - V → WAVEFORM GENERATORS & SPECIAL FUNCTION IC's

R. Sne

Introduction :-

* The op-amps are widely used in circuits for generating various waveforms.

* Analog and digital equipments require one (or) more periodic waveforms for timing, control and other functions.

* The commonly used sinusoidal, square, Triangular Waveform generations are other forms of evolution in the design of operational amplifiers.

* It is capable of generating repetitive waveforms of fixed frequency and amplitude without the need of any other signal.

SINE-WAVE GENERATORS :-

* The sine-wave is one of the most fundamental waveforms.

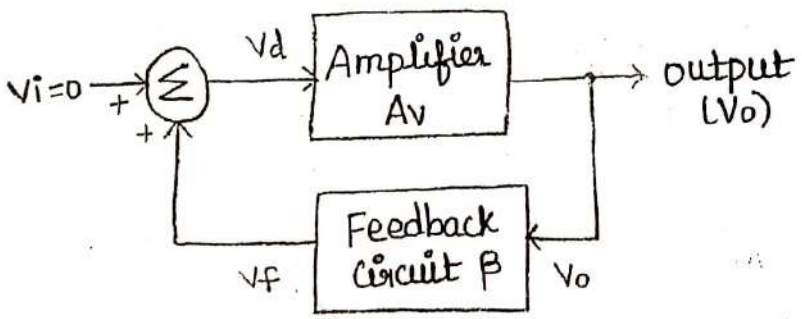
* The sine-wave oscillator using opamp the required phase shift of 180° in the feed back loop.

* It is a Lc or Rc combination.

CONDITIONS FOR OSCILLATIONS :-

* oscillator is also called feedback amplifier.

* The part of output is fed back to the input with the use of a feedback circuit is called oscillator



$V_d = V_f + V_i$

$V_o = A_v V_d = A_v (V_f + V_i)$

$V_f = \beta V_o = \beta A_v (V_f + V_i)$

$V_o = A_v (\beta V_o + V_i)$; $V_o = A_v \beta V_o + A_v V_i$;

$V_o [1 - A_v \beta] = A_v V_i$

$$\therefore \frac{V_o}{V_i} = \frac{A_V}{1 - A_V\beta}$$

$V_i = 0$, $V_o \neq 0$

$|A_V\beta| \geq 1$

$\angle A_V\beta = 0^\circ$ or 360°

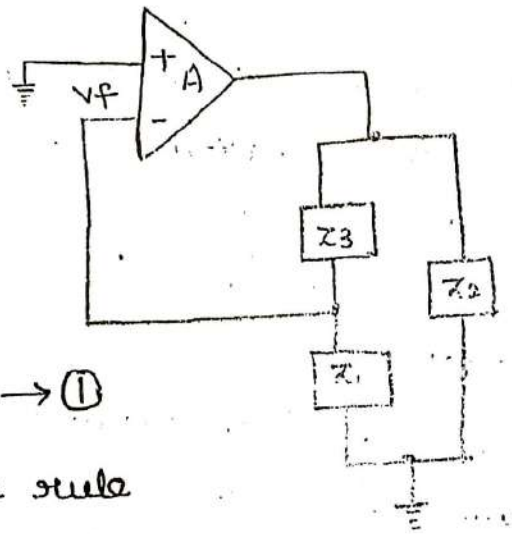
Two Basic requirements for sustained oscillations :-

(i) The magnitude of the loop gain, $A_V\beta$, must be unity

(ii) The total phase-shift of the loop gain, $A_V\beta$, must be equal to 0° or 360°.

LC OSCILLATORS :-

In LC oscillator op-amp is considered. $R_o \neq 0$.



$$\beta = -\frac{V_f}{A_V' f} \rightarrow (1)$$

By voltage divide rule

$$V_f = \frac{Z_1}{Z_1 + Z_3} V_o \longrightarrow (2)$$

Also,

$$V_o = \frac{-Z}{Z + R_o} V_f' A$$

$$\frac{1}{V_f' A} = \frac{-Z}{Z + R_o} \frac{1}{V_o}$$

$$\beta = \frac{-V_f}{A V_f'}$$

$$\beta = \frac{Z_1}{Z_1 + Z_3} \frac{V_o}{V_o} \cdot \frac{Z}{Z + R_o} \frac{1}{V_o}$$

$$= \frac{Z_1 Z}{(Z_1 + Z_3)(Z + R_o)}$$

→ When Lc ckt is applied on Integrals

$\beta \Rightarrow 'j'$

$Z \rightarrow X.$

$$\beta = \frac{Z_1 Z_2}{j(R_0(Z_1+Z_2+Z_3)+Z_2(Z_1+Z_3)}$$

$$\beta = \frac{X_1 X_2}{j R_0(X_1+X_2+X_3)+X_2(X_1+X_3)}$$

When β' is calculated by ω_0

$$\beta = \frac{X_1}{X_2} \rightarrow (4)$$

$$\beta(\omega_0) = \frac{X_1}{X_1+X_3} \rightarrow (5)$$

* $\beta(\omega_0)$ must be positive.
* X_1 & X_2 have same sign.
* X_1 & X_2 are capacitors & X_3 are inductor

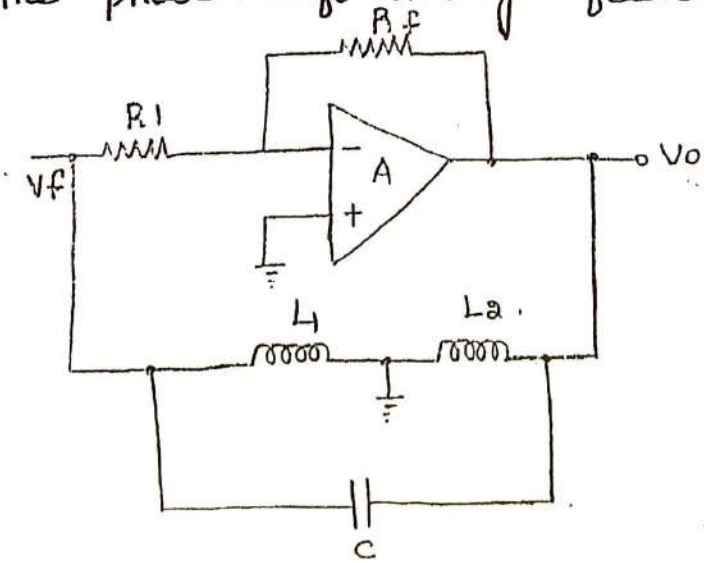
HARTLEY OSCILLATOR:-

→ The op amp is connected to operate in Inverting mode.

→ X_1 & X_2 are ~~capacitive~~ Inductive reactance

→ X_3 is feedback network.

→ The phase shift Through feedback network is 180°.



$X_1 = j\omega L_1$

$X_2 = j\omega L_2.$

$$X_3 = \frac{1}{j\omega C}$$

$$X_3 = -j/\omega C$$

Angular frequency of oscillation

$$\omega_0 = \sqrt{\frac{1}{C(L_1+L_2)}} \quad \text{and} \quad \beta(\omega_0) = \frac{L_1}{L_2}.$$

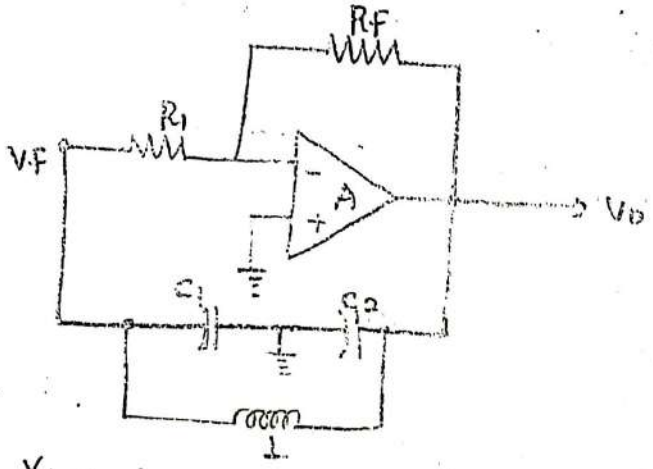
Frequency of oscillation $f_0 = \frac{1}{2\pi\sqrt{C L_T}}$.

Where $L_T = L_1 + L_2$. (or) $L_T = L_1 + L_2 + 2M$

M is the mutual inductance of coils L_1 and L_2.

COLPITTS OSCILLATOR:-

→ The feedback is connected to (-) terminal.
→ The op-amp work as an Inverting Amplifier
→ X_1 & X_2 are capacitive reactance
→ X_3 is Inductive element
→ 180° phase shift.



$$X_1 = \frac{1}{j\omega C_1} = -j/\omega C_1$$

$$X_2 = \frac{1}{j\omega C_2} = -j/\omega C_2.$$

$$X_3 = j\omega L$$

Angular frequency of oscillation ω_0

$$\omega_0 = \sqrt{\frac{1}{L\left(\frac{C_1 C_2}{C_1+C_2}\right)}}$$

$$\beta(\omega_0) = \frac{C_2}{C_1}$$

Frequency of oscillation

$$f_o = \frac{1}{2\pi\sqrt{L C_T}}$$

$$C_T = \frac{C_1 C_2}{C_1 + C_2}$$

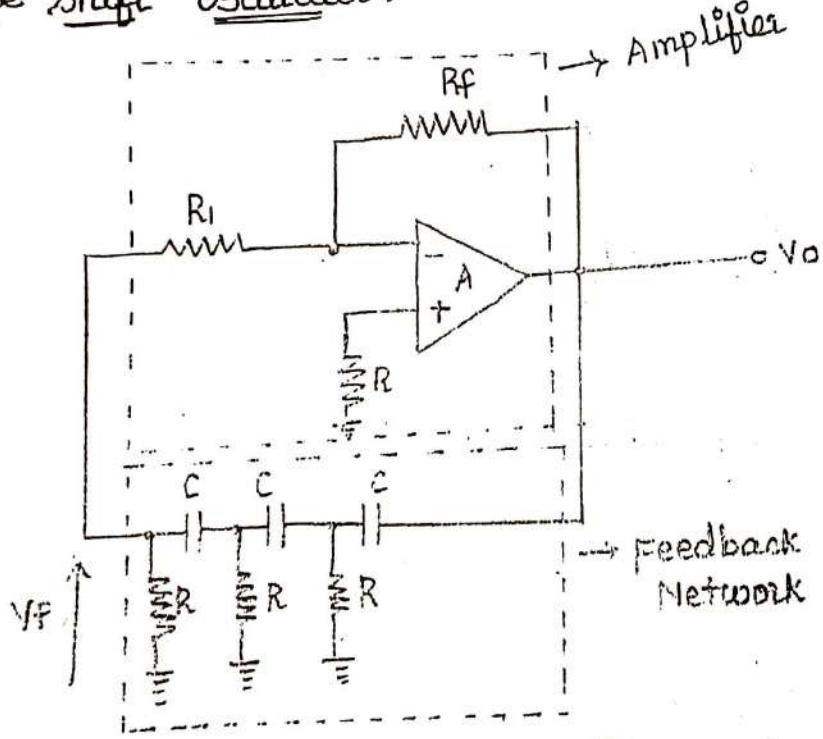
The feedback factor β at the oscillation frequency is -1

RC OSCILLATORS :-

* It operate well at high frequencies.
* At low frequencies inductor and capacitors required for the timing circuit would be very bulky

(i) Rc phase shift oscillator
(ii) Wein bridge oscillator

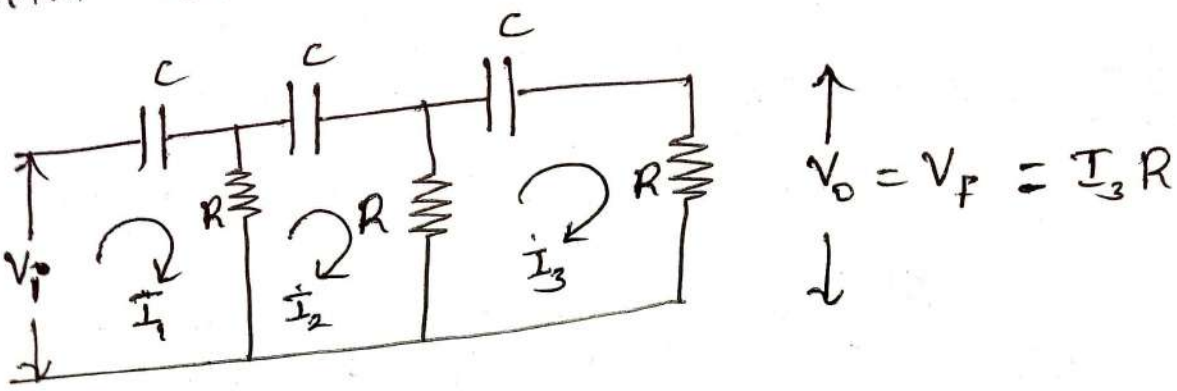
Rc phase shift oscillator :-



RC PHASE SHIFT OSCILLATOR.

* op-amp is used in Inverting configuration.
* It produces 180° phase-shift at the output.
* The total phase shift around the loop is 360° or 0°
* gain of the amplifier is large and in series Rc Network is exactly 180°

Derivation of Frequency of Oscillator:



Apply KVL in Loop 1:

$$\frac{1}{j\omega C} I_1 + R[I_1 - I_2] = V_i$$

$$\left[R + \frac{1}{j\omega C}\right] I_1 - I_2 R = V_i \longrightarrow (1)$$

Apply KVL in Loop 2:

$$\frac{1}{j\omega C} I_2 + R[I_2 - I_1] + R[I_2 - I_3] = 0$$

$$\frac{1}{j\omega C} I_2 + I_2 R - I_1 R + I_2 R - I_3 R = 0$$

$$-I_1 R + I_2\left[\frac{1}{j\omega C} + 2R\right] - I_3 R = 0 \longrightarrow (2)$$

Apply KVL in Loop 3:

$$\frac{1}{j\omega C} I_3 + R[I_3 - I_2] + R I_3 = 0$$

$$\frac{1}{j\omega C} I_3 + I_3 R - I_2 R + I_3 R = 0$$

$$-I_2 R + I_3\left\{\frac{1}{j\omega C} + 2R\right\} = 0 \longrightarrow (3)$$

Replace $s=jw$ in eq ①, ② & ③

$$\left\{R+\frac{1}{sc}\right\} I_1 - I_2 R = V_i \longrightarrow ④$$

$$-I_1 R + I_2 \left\{\frac{1}{sc} + 2R\right\} - I_3 R = 0 \longrightarrow ⑤$$

$$-I_2 R + I_3 \left\{\frac{1}{sc} + 2R\right\} = 0 \longrightarrow ⑥$$

Matrix

$$\begin{bmatrix} R+1/sc & -R & 0 \\ -R & 1/sc+2R & -R \\ 0 & -R & 1/sc+2R \end{bmatrix} \begin{bmatrix} I_1 \\ I_2 \\ I_3 \end{bmatrix} = \begin{bmatrix} V_i \\ 0 \\ 0 \end{bmatrix}$$

Output Voltage : $V_0 = V_f = I_3 R$

$$I_3 = \frac{\Delta_3}{\Delta}$$

By Cramer's Rule,

$$\Delta = \begin{bmatrix} R+1/sc & -R & 0 \\ -R & 1/sc+2R & -R \\ 0 & -R & 1/sc+2R \end{bmatrix}$$

$$= \begin{bmatrix} \frac{1+sRC}{sC} & -R & 0 \\ -R & \frac{1+2sRC}{sC} & -R \\ 0 & -R & \frac{1+2sRC}{sC} \end{bmatrix}$$

$$\Delta = \frac{1+RSC}{SC}\left\{\left(\frac{1+2SCR}{SC}\right)^2 - R^2\right\} + R\left\{(-R)\left(\frac{1+2SRC}{SC}\right) - 0\right\}$$

$$+0\left\{R^2 - 0\right\}$$

$$= \frac{(1+SRC)(1+2SRC)^2}{(SC)^3} - R^2\left(\frac{1+SRC}{SC}\right) - R^2\left(\frac{1+2SRC}{SC}\right)$$

$$= \frac{(1+SRC)(1+2SRC)^2 - R^2(1+SRC)(SC)^2 - R^2(1+2SRC)(SC)^2}{(SC)^3}$$

$$= \frac{(1+SRC)(1+4S^2R^2C^2+4SRC) - R^2(SC)^2(1+SRC) - R^2(SC)^2(1+2SRC)}{(SC)^3}$$

$$= \frac{(1+4S^2R^2C^2+4SRC+SRC+4S^3R^3C^3+4S^2R^2C^2 - R^2S^2C^2 - R^3S^3C^3 - R^2S^2C^2 - 2S^3R^3C^3)}{S^3C^3}$$

$$\Delta = \frac{1+5SRC+6S^2R^2C^2+S^3R^3C^3}{S^3C^3} \longrightarrow (7)$$

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$$\Delta_3 = \begin{bmatrix} \frac{1+SRC}{SC} & -R & V_i \\ -R & \frac{1+2SRC}{SC} & 0 \\ 0 & -R & 0 \end{bmatrix}$$

$$= \left(\frac{1+SRC}{SC}\right)\left\{0-0\right\} + R\left\{0-0\right\} + V_i\left\{R^2-0\right\}$$

$$\Delta_3 = 0 + 0 + V_i R^2$$

$$\Delta_3 = V_i R^2 \longrightarrow (8)$$

The current flow in loop 3;

$$I_3 = \frac{\Delta_3}{\Delta}$$

$$I_3 = \frac{V_i R^2}{\frac{1+5SRC+6S^2R^2C^2+S^3R^3C^3}{S^3C^3}}$$

$$I_3 = \frac{V_i R^2 S^3 C^3}{1+5SRC+6S^2R^2C^2+S^3R^3C^3} \longrightarrow (9)$$

Output Voltage V_o,

$$V_o = V_f = I_3 R$$

Sub (9) $$V_o = \frac{V_i R^3 S^3 C^3}{1 + 5SRC + 6S^2R^2C^2 + S^3R^3C^3}$$

$$\beta = \frac{V_o}{V_i} = \frac{S^3R^3C^3}{1 + 5SRC + 6S^2R^2C^2 + S^3R^3C^3}$$

Replace $S = j\omega$,

$$\beta = \frac{(j\omega)^3 R^3 C^3}{1 + 5(j\omega)RC + 6(j\omega)^2R^2C^2 + (j\omega)^3R^3C^3}$$

$$\beta = \frac{-j\omega^3 R^3 C^3}{1 + 5j\omega RC - 6\omega^2R^2C^2 - j\omega^3R^3C^3}$$

divide by $-j\omega^3R^3C^3$ in Nr & Dr

$$\beta = \frac{1}{\frac{1}{-j\omega^3R^3C^3} + \frac{5j\omega RC}{-j\omega^3R^3C^3} - \frac{6\omega^2R^2C^2}{-j\omega^3R^3C^3} - \frac{j\omega^3R^3C^3}{-j\omega^3R^3C^3}}$$

$$= \frac{1}{-\frac{1}{j\omega^3R^3C^3} - \frac{5}{\omega^2R^2C^2} + \frac{6}{j\omega RC} + 1}$$

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Assume, $\alpha = \frac{1}{\omega RC}$

$$\beta = \frac{1}{+j\alpha^3 - 5\alpha^2 - j6\alpha + 1}$$

$$\beta = \frac{1}{(1-5\alpha^2) - j\alpha(6-\alpha^2)}$$

Imaginary part = 0

$$-j\alpha(6-\alpha^2) = 0$$

$$6 - \alpha^2 = 0$$

$$\alpha^2 = 6$$

$$\alpha = \sqrt{6}$$

$$\frac{1}{\omega RC} = \sqrt{6}$$

$$\frac{1}{2\pi FRC} = \sqrt{6}$$

$$\boxed{f = \frac{1}{2\pi\sqrt{6}RC}}$$

Real Part,

$$\beta = \frac{1}{1-5\alpha^2} = \frac{1}{1-5(\sqrt{6})^2}$$

$$\beta = \frac{1}{1-30} = \frac{1}{-29}$$

$$\boxed{|\beta| = 1/29}$$

Condition of oscillator

$$|A\beta| \geq 1$$

$$|A||\beta| \geq 1$$

$$|A|\left|\frac{1}{29}\right| \geq 1$$

$$|A| \geq 29$$

To make $|A| \geq 29$, $R_f = 29$ times of R_1.

Advantages:

* circuit is simple to design.
* It produces sinusoidal o/p waveform.
* It is fixed frequency oscillator.

Disadvantages:

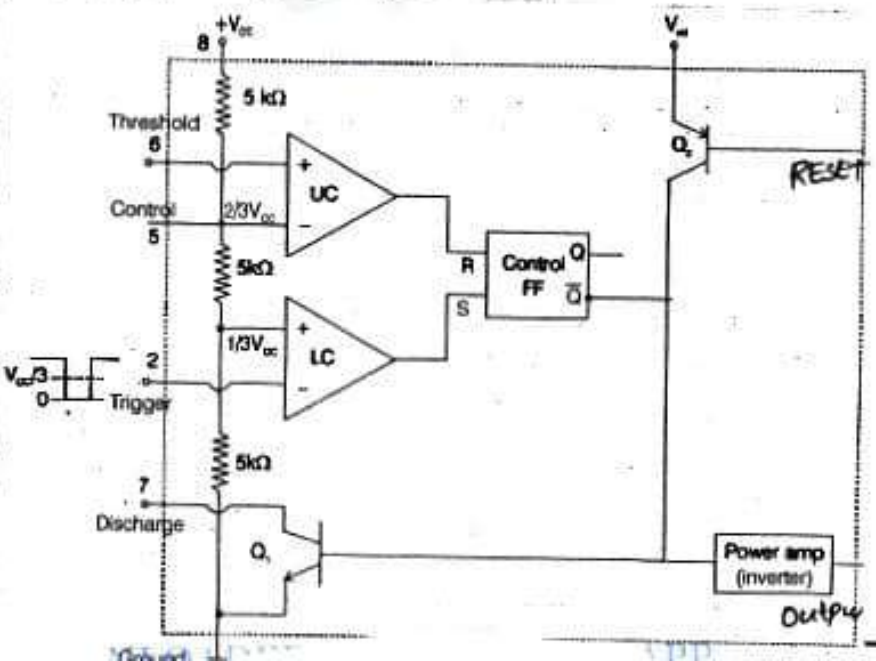
* frequency stability is poor.

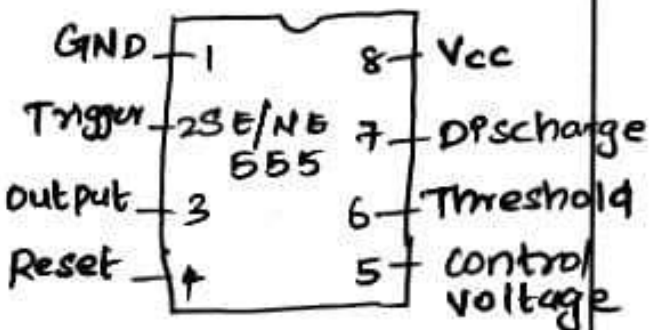
TIMER IC 555 and its modes of multivibrator and explain on it?

* 555 timer is a highly stable device for generating accurate time delay(or) oscillation.
* A single 555 timer can provide time delay ranging from microseconds to hours where as counter timer can have a maximum timing range of days.
* It is designed to perform signal generation and specific timing
* Voltage range: +5V to +18V
* drive load : 200mA
* It is compatible with both TTL and CMOS logic circuits and op-amp based circuits

APPLICATIONS:

1. oscillator
2. pulse generator
3. Ramp and saluare wave generator
4. Monoshot multivibrator
5. Burglar alarm
6. Traffic light control
7. Voltage monitor





PIN DIAGRAM OF IC 555

* The positive d.c power supply terminal is connected to pins (Vcc) and negative terminal is connected to pin 1 (GND)

* A control voltage input terminal accepts a modulation control input voltage applied externally.

* The (+) input terminal of the upper comparator is called threshold terminal

* The (-) input terminal of the Lower comparator is called trigger terminal.

OPERATION:

* In Standby mode, the output $\bar{Q}$ of the control FF is HIGH. This makes the output low because of power amplifier which is basically an inverter.

* When a negative going trigger pulse is applied to pin 2 and should have its dc level greater than the threshold level of the lower comparator.

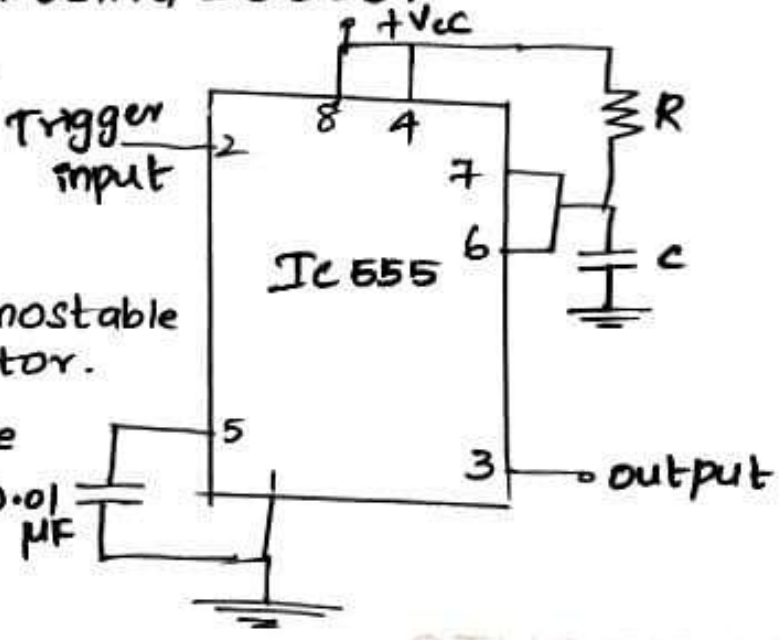
* At the negative going edge of the trigger, as the trigger passes through the output of the lower comparator goes HIGH and sets the control FF.

MONOSTABLE MULTIVIBRATOR USING IC 555:

* The Monostable multivibrator has one stable state and one-quest stable state.

* It is also known as monostable (or) one-shot multivibrator.

* It remains in its Stable state until an impulse pulse triggers it into its quasi-stable state.



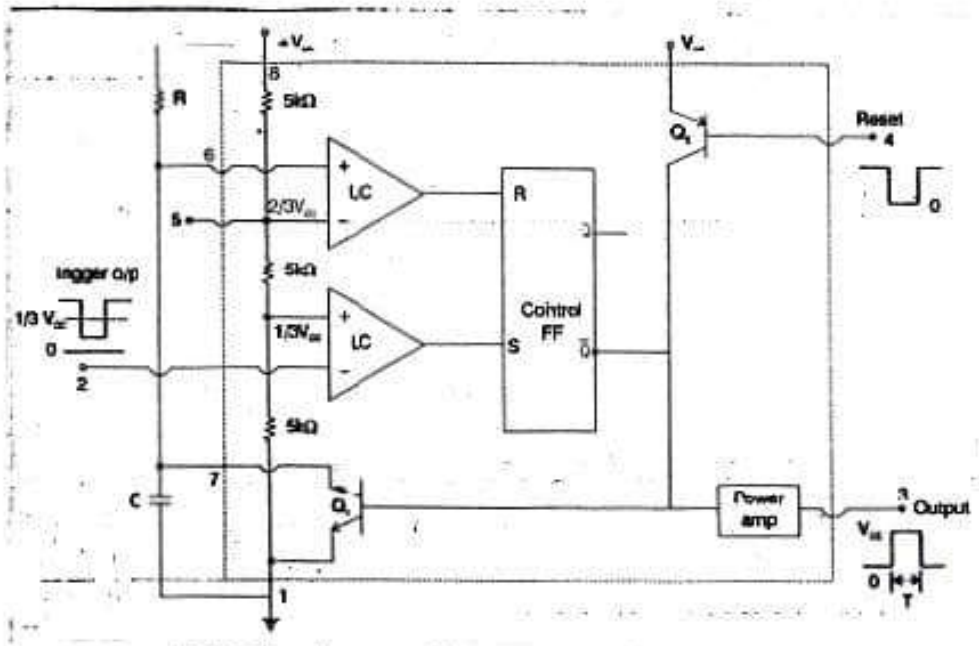


Fig.4.4 Timer in mono-stable operation with functional diagram

* In the standby mode, control FF holds transistor Q_1 ON, thus clamping the external timing capacitor C to ground.

ANALYSIS:

Voltage across the capacitor as given below:

$$V_C = V_{CC}\left(1 - e^{-t/RC}\right)$$

At $t = T$, $V_C = \frac{2}{3} V_{CC}$

$$\frac{2}{3} V_{CC} = V_{CC}\left(1 - e^{-T/RC}\right)$$

$$\frac{2}{3} = 1 - e^{-T/RC}$$

$$\frac{2}{3} - 1 = -e^{-T/RC}$$

$$\frac{-1}{3} = -e^{-T/RC}$$

Taking natural log on both sides

$$\ln\left(\frac{1}{3}\right) = \frac{-T}{RC}$$

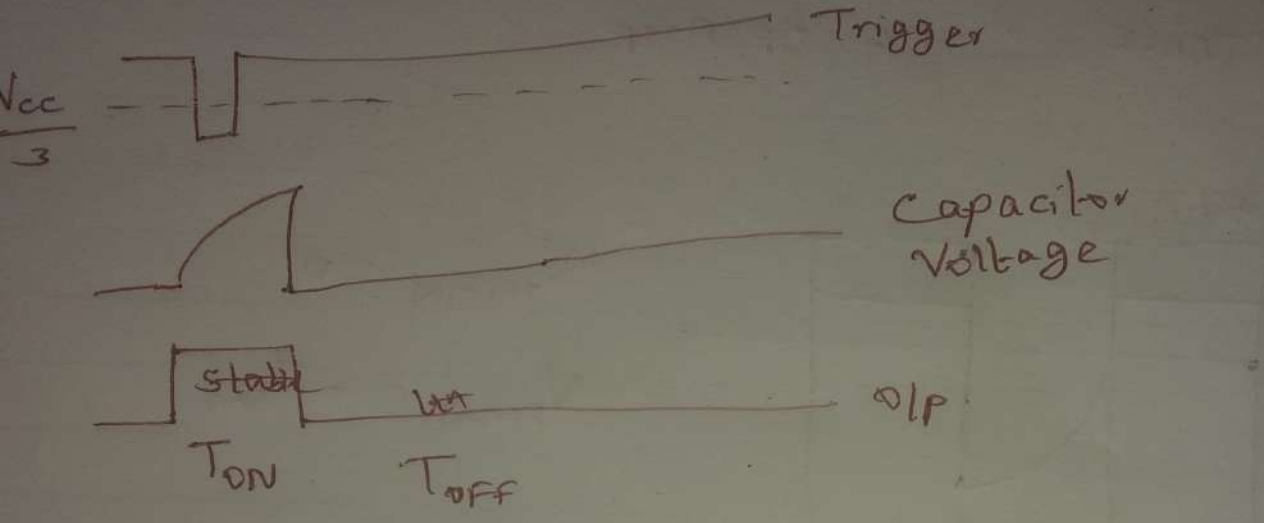
$$-T = RC \ln\left(\frac{1}{3}\right)$$

$$\boxed{T = 1.1\,RC}$$

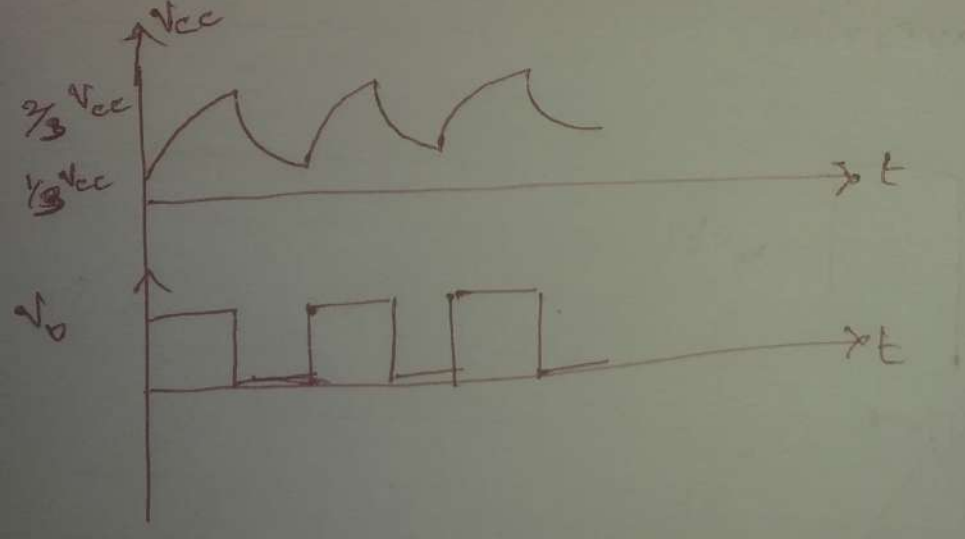
APPLICATIONS MULTIVIBRATOR USING 555:

(a) Pulse missing Detector
(b) Freqluency divider
(c) PWM application

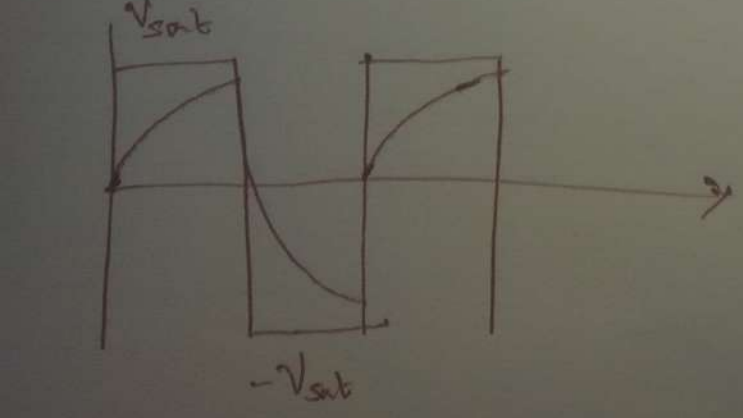
MONOSTABLE USING IC 555:



ASTABLE USING IC555:



Astable using Op-Amp:



$V_{Final} = +V_{sat}$

$V_{initial} = -\beta V_{sat}$

ASTABLE MULTIVIBRATOR USING IC 555:

* comparing with monostable operation, the timing resistors is now split into two sections R_A and R_B.
* The discharge (pin 7) terminal is connected to the junction of R_A and R_B.
* Threshold (pin 6) and trigger (pin 2) terminals are connected to the VC terminal and control (pin 5) terminal is by passed to ground through 0.01 μF capacitor.

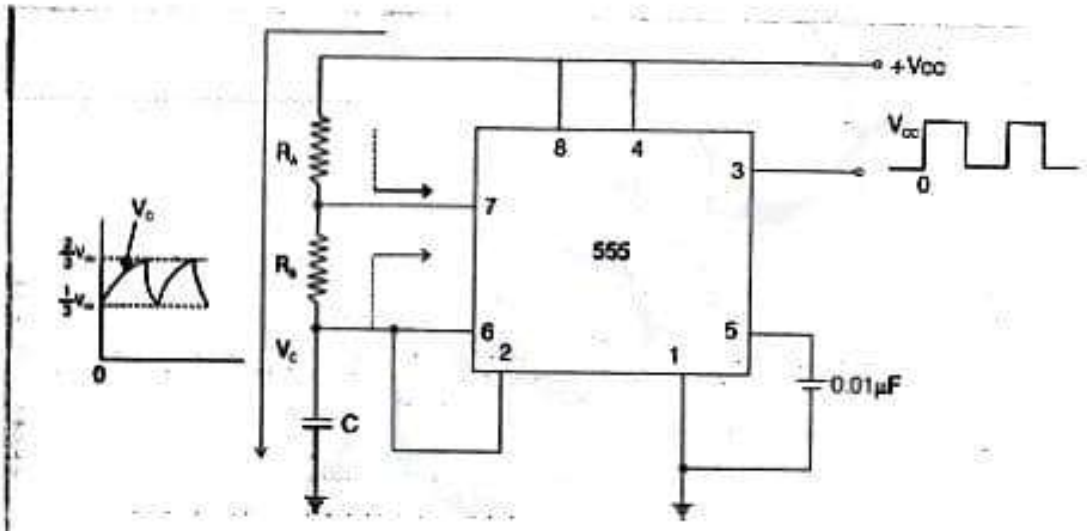


Fig.4.12 Astable multivibrator

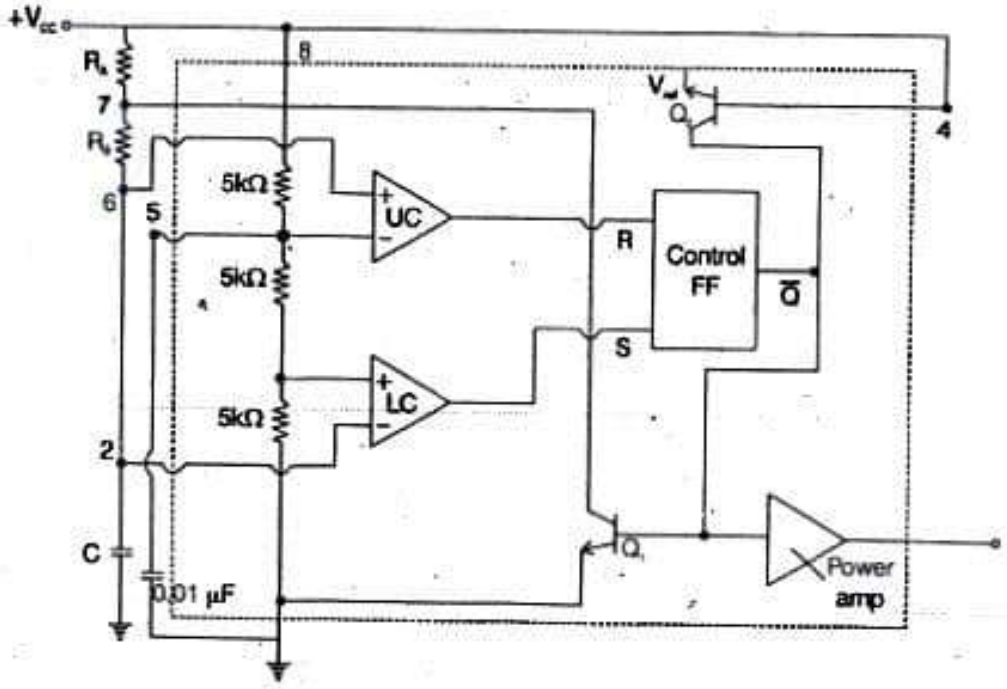


Fig.4.13 Functional diagram of astable multivibrator using 555 timer

* When the capacitor voltage reaches and rises above $\frac{2}{3}V_{cc}$ the upper comparators triggers and reset the control flipflop so that $\bar{Q} = 1$.

* Q_1 transistor → ON

* Capacitor starts discharging towards ground through R_B and transistor Q_1 with the time constant time $R_B C$.

* During the discharge of timing capacitor C as it reaches $\frac{V_{cc}}{3}$, the lower comparators is triggered and this stage S=1, R=0 which turns $\bar{Q} = 0$.

* The capacitor is charged and discharged between $\frac{2}{3}V_{cc}$ and $\frac{1}{3}V_{cc}$ respectively.

ANALYSIS:

$$V_c = V_{cc}(1 - e^{-t/RC})$$

$t = t_1$, $V_c = \frac{2}{3}V_{cc}$

$$\frac{2}{3}V_{cc} = V_{cc}(1 - e^{-t_1/RC})$$

$$\frac{2}{3} = 1 - e^{-t_1/RC}$$

$$\frac{2}{3} - 1 = -e^{-t_1/RC}$$

$$-\frac{1}{3} = -e^{-t_1/RC}$$

Taking natural log on both sides

$$\ln\left(\frac{1}{3}\right) = \frac{-t_1}{RC}$$

$$-t_1 = RC \ln\left(\frac{1}{3}\right)$$

$$\boxed{t_1 = 1.1RC}$$

At $t = t_2$, $V_C = \frac{1}{3} V_{CC}$

$$\frac{1}{3} V_{CC} = V_{CC}\left(1 - e^{-t_2/RC}\right)$$

$$\frac{1}{3} - 1 = -e^{-t_2/RC}$$

$$\frac{-2}{3} = -e^{-t_2/RC}$$

Taking natural log on both sides

$$\ln\left(\frac{2}{3}\right) = \frac{-t_2}{RC}$$

$$-t_2 = RC \ln\left(\frac{2}{3}\right)$$

$$\boxed{t_2 = 0.405\ RC}$$

$$t_{High} = t_1 - t_2$$

$$= 1.1RC - 0.405\,RC$$

$$= RC(1.1 - 0.405)$$

$$\boxed{t_{HIGH} = 0.69\ RC}$$

So for the given circuit

$$t_{High} = 0.69\,(R_A + R_B)\,C$$

$$t_{low} = 0.69\,R_B\,C$$

$$T = t_{HIGH} + t_{LOW}$$

$$= 0.69\,(R_A + R_B)\,C + 0.69\,R_B\,C$$

$$= 0.69\,R_A C + 0.69\,R_B C + 0.69\,R_B C$$

$$T = 0.69\,(R_A + 2R_B)\,C$$

$$f = \frac{1}{T} = \frac{1.45}{(R_A + 2R_B)C}$$

The duty cycle D of the circuit is defined as the ratio of ON time to the total time period.

$$T = (t_{ON} + t_{OFF})$$

*In this circuit, when the transistor Q_1 is on the output goes low.

$$D\% = \frac{t_{low}}{T} \times 100$$

$$D\% = \frac{R_B}{R_A + 2R_B} \times 100$$

APPLICATIONS IN ASTABLE MODE:

* FSK Generator
* Timer as a schmitt trigger.

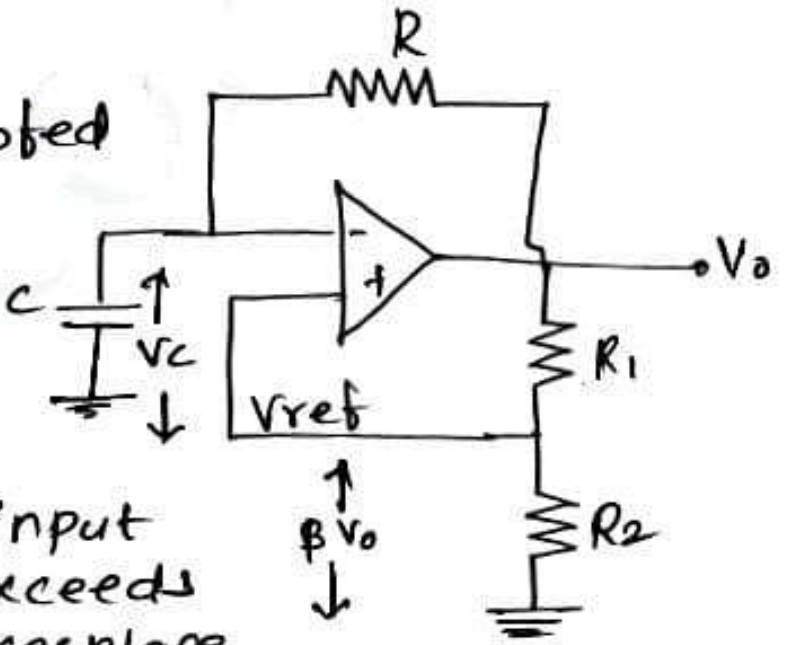
SQUARE WAVE GENERATORS:

* Besides generating sine waves, the op-amp generates saluare waveform and pulses, an active device generate a saluare waveform ps also called as multivibrator

(i) Astable multivibrator

* It is also called as free running oscillator, the principle of generation of saluare wave output is to force an op-amp to operate in the saturation region.

$$\beta = \frac{R_2}{R_1 + R_2}$$



* The output is also fed back to inverting terminal input after integrating by lowpass RC combination.
* whenever the input at (-) input just exceeds Vref switching takes place to + Vsat to − Vsat.

$$V_c(t) = V_f + (V_i - V_f)\, e^{-t/RC}$$

$V_f = +V_{sat}$

$V_i = -\beta V_{sat}$

considering

$$V_c(t) = V_{sat} + (-\beta V_{sat} - V_{sat})\, e^{-t/RC}$$

at $t = T_1$

$$V_c(t) = +\beta V_{sat}$$

$$\beta V_{sat} = V_{sat} - (\beta V_{sat} + V_{sat})\, e^{-T_1/RC}$$

$$\beta V_{sat} - V_{sat} = -V_{sat}(1+\beta)\, e^{-T_1/RC}$$

$$V_{sat}(\beta - 1) = -V_{sat}(1+\beta)\, e^{-T_1/RC}$$

$$V_{sat}(1-\beta) = V_{sat}(1+\beta)\, e^{-T_1/RC}$$

$$e^{-T_1/RC} = \frac{1-\beta}{1+\beta}$$

Taking log on both sides

$$\ln\left(\frac{-T_1}{RC}\right) = \ln\left(\frac{1-\beta}{1+\beta}\right)$$

Considering $\beta = 0.5$

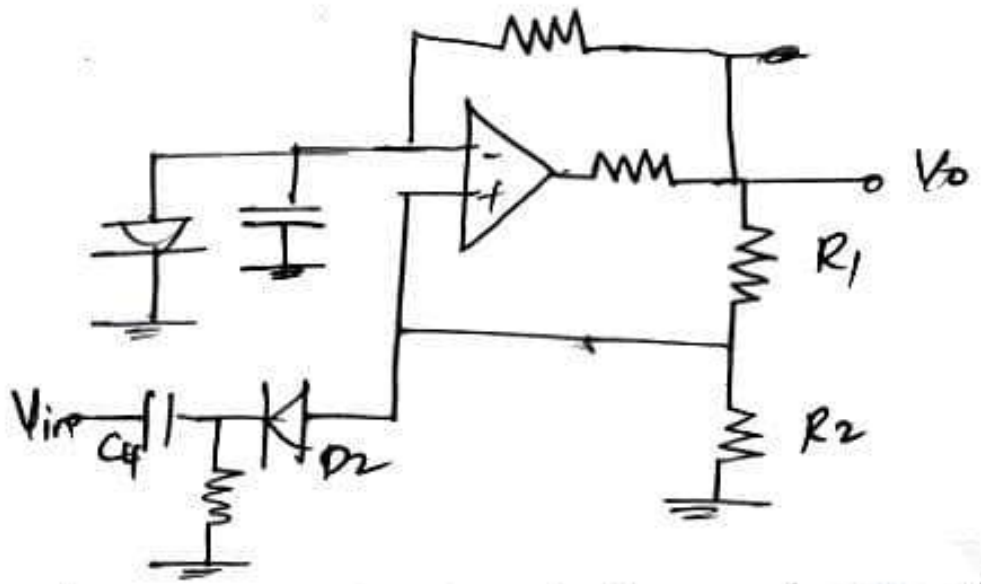
$$\frac{-T_1}{RC} = \ln\left(\frac{1-0.5}{1+0.5}\right)$$

$$\frac{-T_1}{RC} = \ln\left(\frac{0.5}{1.5}\right)$$

$$\frac{-T_1}{RC} = \ln\left(\frac{1}{3}\right)$$

$$\boxed{T_1 = 1.1\,RC}$$

(ii) MONOSTABLE MULTIVIBRATOR:



* It has one stable state and one aluasi stable state.
* This circuit is useful for generating single output pulse of adjustable time duration in response to a triggering signal.
* The width of output signal depends only on external components connected to the op-amp
* Diode D_1 clamps the capacitor voltage to 0.7V when output is +Vsat.
* A negative going pulse signal of magnitude V_i passing through differentiator R_4 C_4 and diode D_2 produces going triggering impulse and is applied to the (+) input terminal.

$$V_o = V_f + (V_i - V_f) e^{-t/RC}$$

$$V_f = -V_{sat}$$

$$V_i = V_D$$

$$V_o = -V_{sat} + [V_D + V_{sat}) e^{-t/RC}$$

At $t = T$, $V_o = -\beta V_{sat}$

$$-\beta V_{sat} = -V_{sat}(V_D + V_{sat})e^{-T/RC}$$

$$-\beta V_{sat} + V_{sat} = (V_D + V_{sat})e^{-T/RC}$$

$$\frac{V_{sat}(1-\beta)}{V_D + V_{sat}} = e^{-T/RC}$$

$$\frac{V_{sat}(1-\beta)}{V_{sat}\left(1+\frac{V_D}{V_{sat}}\right)} = e^{-T/RC}$$

$$-\frac{T}{RC} = \ln\left(\frac{1 + V_D/V_{sat}}{1-\beta}\right)$$

$$T = RC \ln(1-\beta)$$

$V_{sat} >> V_D$

$R_1 = R_2$

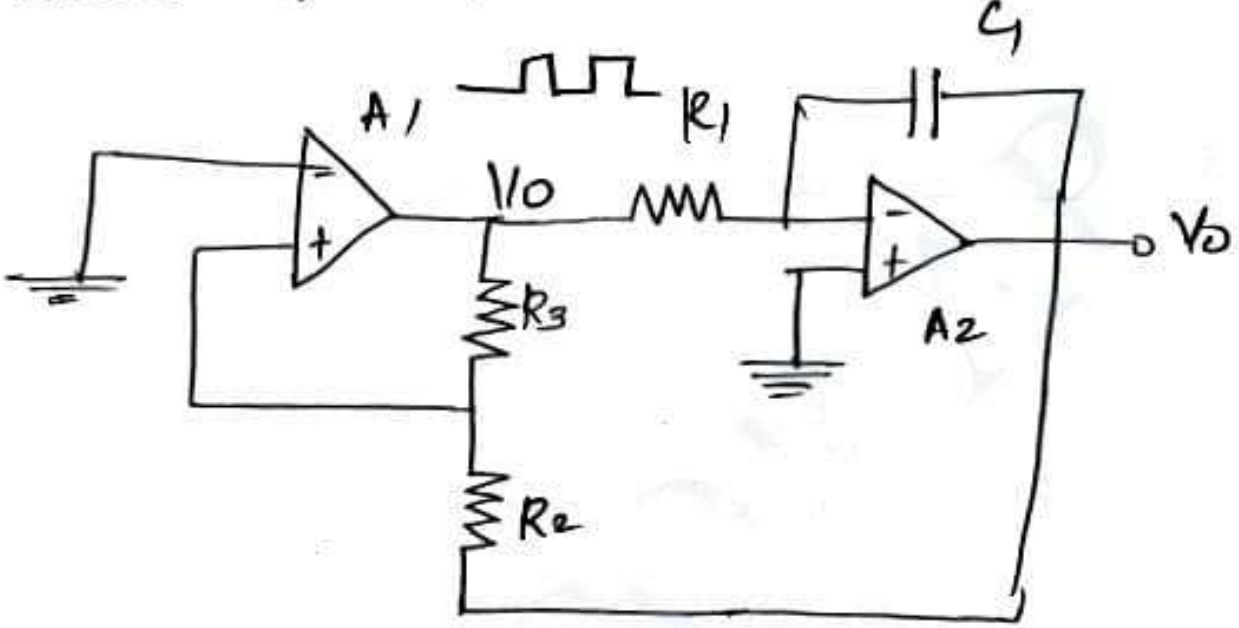
$\beta = 0.5$

$$\boxed{T = 0.69RC}$$

* Monostable multivibrator circuit is also referred as time delay circuit as it generates a fast transition at a predetermined time T after the application of input trigger

TRIANGULAR WAVE GENERATOR:

* Generally triangular wave generator may be derived from other sources through the use of comparators.
* Linear wave forms such as triangle and ramp may be derived from the charge/discharge action of a capacitor.



* It basically consists of two level comparator followed by integrator circuit. The output of A_1 is a saluare wave of amplitude $\pm V_{sat}$ and is applied to the (-) i/p of the integrator producing a triangular wave.

$$P = V_f + (V_i - V_f)\beta$$

$$V_f = -V_{ramp}$$

$$V_f = +V_{sat}$$

$$\beta = \frac{R_2}{R_2 + R_3}$$

$$P = -V_{ramp} + (V_{sat} + V_{ramp})\frac{R_2}{R_2 + R_3}$$

At; $t = t_1$, voltage at p becomes equal to zero

$$-V_{ramp} = -\frac{R_2}{R_3}(+V_{sat}) \quad \text{—— (1)}$$

at $t = t_2$, when output of A_1 switches from $-V_{sat}$ to $+V_{sat}$

$$V_{ramp} = -\frac{R_2}{R_3}(-V_{sat}) \quad \text{—— (2)}$$

Peak to peak value of output is

$$V_{o(pp)} = +V_{ramp} - (-V_{ramp})$$

$$V_{o(pp)} = 2\frac{R_2}{R_3}V_{sat} \quad \text{—— (3)}$$

The output from $-V_{ramp}$ to $+V_{ramp}$ in half the time period $T/2$

$$V_o = \frac{-1}{RC}\int V_i\,dt$$

$$V_{o(pp)} = \frac{-1}{R_1C_1}\int_0^{T/2}(+V_{sat})\,dt$$

$$= \frac{V_{sat}}{R_1C_1}\left(\frac{T}{2}\right)$$

$$T = 2R_1C_1\frac{V_{o(pp)}}{V_{sat}} \quad \text{—— (4)}$$

Putting $V_{o(pp)}$ value

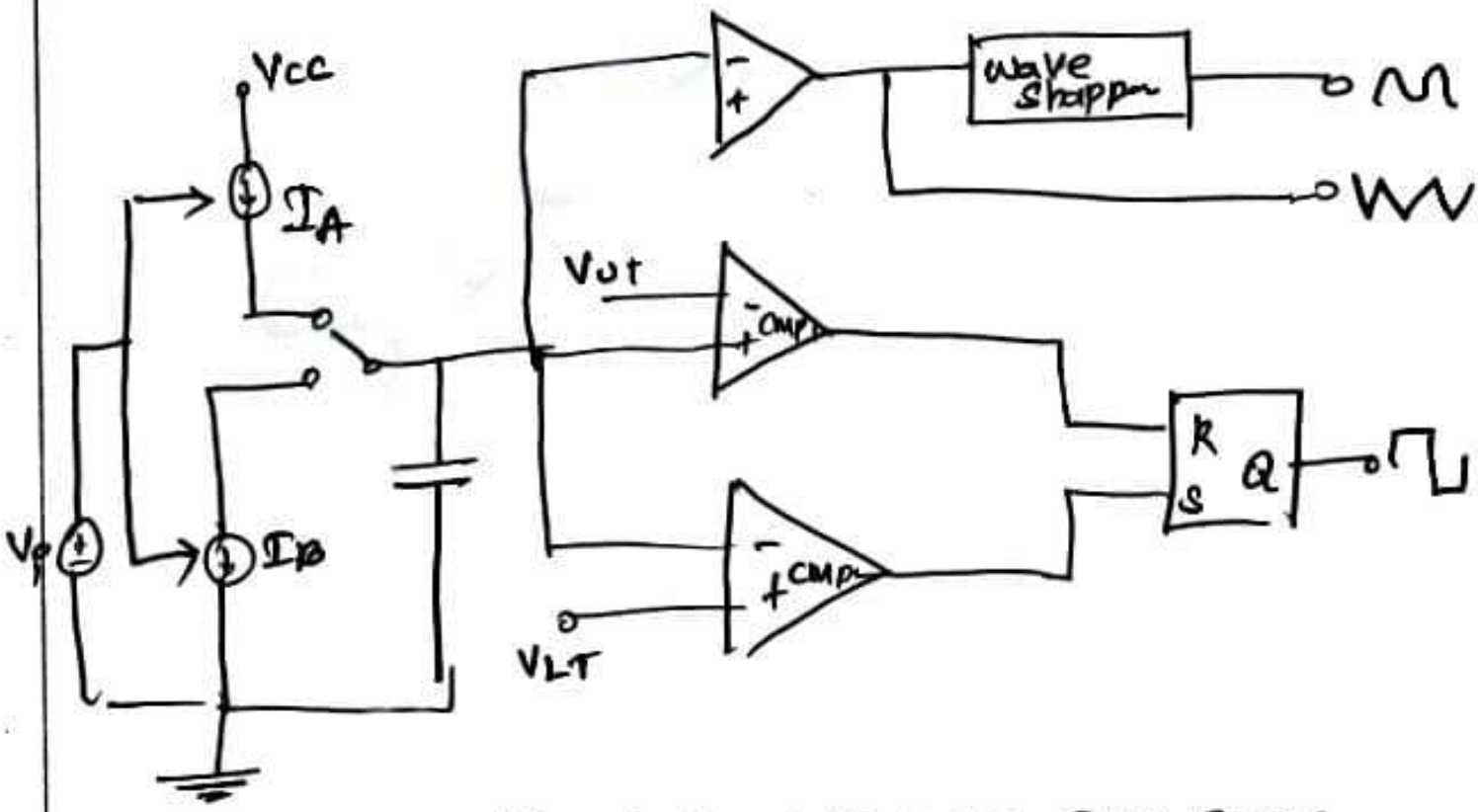
$$T = 2R_1C_1\frac{2\frac{R_2}{R_3}V_{sat}}{V_{sat}}$$

$$= \frac{4R_1C_1R_2}{R_3}$$

$$\boxed{f_o = \frac{1}{T} = \frac{R_3}{4R_1C_1R_2}}$$

ICL 8038 FUNCTION GENERATOR:

* Function generators are designed to provide the basic waveforms such as saluare wave, triangular wave and sine wave.
* They are also called as waveform generators.
* The operation of ICL 8038 is based on charging and discharging of a grounded capacitor C, whose charging and discharging rates are controlled by programmable current generators I_A and I_B respectively
* When switch is at position A, the capacitor charges at a rate determined by current source I_A.
* once the capacitor voltage reaches the threshold value V_{UT} switch position to change from position A to B.



BLOCK DIAGRAM OF ICL 8038 FUNCTION GENERATOR

FREQUENCY OF OUTPUT WAVEFORM:

$$f_{out} = \frac{1}{T}$$

$$T = T_C + T_d$$

$$T_C = \Delta V_C \times \frac{1}{\text{charging current}} \times C$$

$I = \frac{V}{R}$

$$T_C = \frac{V_{CC}}{3} \times \frac{R_A}{V_i} \times C$$

$$\boxed{T_C = \frac{R_A C V_{CC}}{3 V_i}}$$

The discharging time T_d can be given as

$$T_d = \Delta V \times \frac{1}{\text{discharging current}} \times C$$

$$= \frac{V_{CC}}{3} \times \frac{1}{\left(\frac{2V_i}{R_B} - \frac{V_i}{R_A}\right)} \times C$$

$$= \frac{V_{CC}}{3} \times \frac{1}{\frac{2V_i R_A - V_i R_B}{R_A R_B}} \times C$$

$$= \frac{V_{CC} \times R_A R_B \times C}{3 (2V_i R_A - V_i R_B)}$$

$$= \frac{V_{CC}}{3V_i} \times \frac{R_A R_B}{(2R_A - R_B)} \times C$$

$$T_d = \frac{CR_A V_{CC}}{3V_i}\left(\frac{R_B}{2R_A - R_B}\right)$$

$$T = T_C + T_d$$

$$= \frac{CR_A V_{CE}}{3V_i} + \frac{CR_A V_{CE}}{3V_i}\left(\frac{R_B}{2R_A - R_B}\right)$$

$$= \frac{CR_A V_{CC}}{3V_i}\left[1 + \frac{R_B}{2R_A - R_B}\right]$$

$$= \frac{CR_A V_{CC}}{3V_i}\left[\frac{2R_A - R_B + R_B}{2R_A - R_B}\right]$$

$$T = \frac{R_A C V_{CC}}{3V_i}\left[\frac{2R_A}{2R_A - R_B}\right]$$

$$f_{out} = \frac{1}{T}$$

$$= \frac{3V_i}{R_A C V_{CC}}\left(\frac{2R_A - R_B}{2R_A}\right)$$

Duty cycle is given as

$$\% d = \frac{T_C}{T_C + T_d} \times 100$$

$$= \frac{\frac{C R_A V_{CC}}{3V_i}}{\frac{C R_A V_{CC}}{3V_i} + \frac{C R_A V_{CC}}{3V_i}\left(\frac{R_B}{2R_A - R_B}\right)} \times 100$$

$$= \frac{C R_A V_{CC}/3V_i}{\frac{C R_A V_{CC}}{3V_i}\left(1 + \frac{R_B}{2R_A - R_B}\right)}$$

$$= \frac{1}{\frac{2R_A - R_B + R_B}{2R_A - R_B}}$$

$$= \frac{2R_A - R_B}{2R_A} \times 100$$

$$\boxed{\%\ d = \left(1 - \frac{R_B}{2R_A}\right) \times 100}$$

Specifications:

Supply Voltage: ± 18V or 36V

Power dissipation: 750 mW

Input Voltage: max of supply voltage level

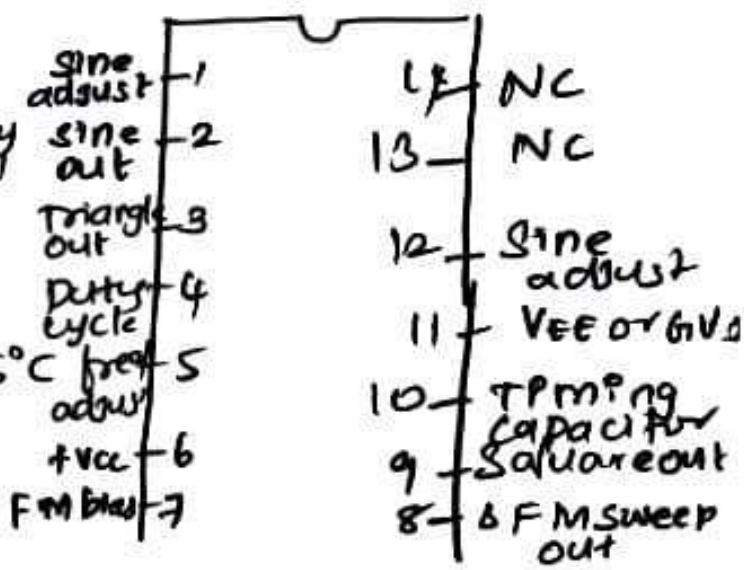
Input Current: 25 mA

output sink current : 25 mA

Storage temperature range : 65°C to 125°C

Distortion: 1%

Linearity: 0.1%



Saw-Tooth Wave Generator:

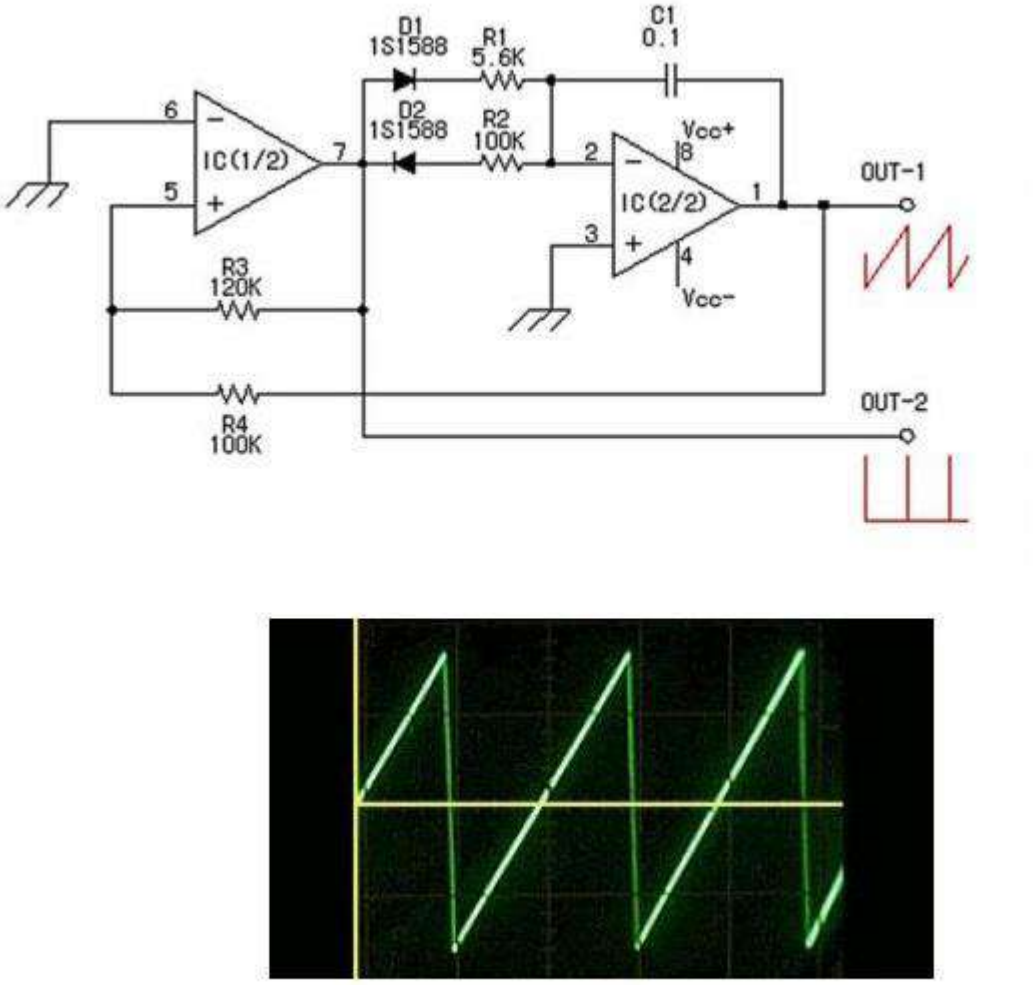


Fig. 5.13 Saw-Tooth Wave Generator Circuit Diagram and output waveform

The saw tooth wave oscillator which used the operational amplifier. The composition of this circuit is the same as the triangular wave oscillator basically and is using two operational amplifiers.

At the circuit diagram above, IC(1/2) is the Schmitt circuit and IC(2/2) is the Integration circuit. The difference with the triangular wave oscillator is to be changing the time of the charging and the discharging of the capacitor. When the

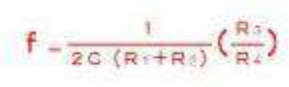
output of IC (1/2) is positive voltage, it charges rapidly by the small resistance (R1) value.

(When the integration output voltage falls) When the output of IC(1/2) is negative voltage, it is made to charge gradually at the big resistance(R2) value. The output waveform of the integration circuit becomes a form like the tooth of the saw. Such voltage is used for the control of the electron beam (the scanning line) of the television,

When picturing a picture at the cathode-ray tube, an electron beam is moved comparative slow. (When the electron beam moves from the left to the right on the screen). When turning back, it is rapidly moved.(When moving from the right to the left).

Like the triangular wave oscillator, the line voltage needs both of the positive power supply and the negative power supply. Also, to work in the oscillation, the condition of R3>R4 is necessary. However, when making the value of R4 small compared with R3, the output voltage becomes small. The near value is good for R3 and R4

The oscillation frequency can be calculated by the following formula.



With the circuit diagram,the oscillation frequency is as follows.

f = (1/2C (R1+R2))*(R3/R4)

= $(1/(2x0.1x10^{-6}x(5.6x10^{3}+100x10^{3}))x(120x10^{3}/100x10^{3})$

= $(1/(21.12x10^{-3}))x1.2$

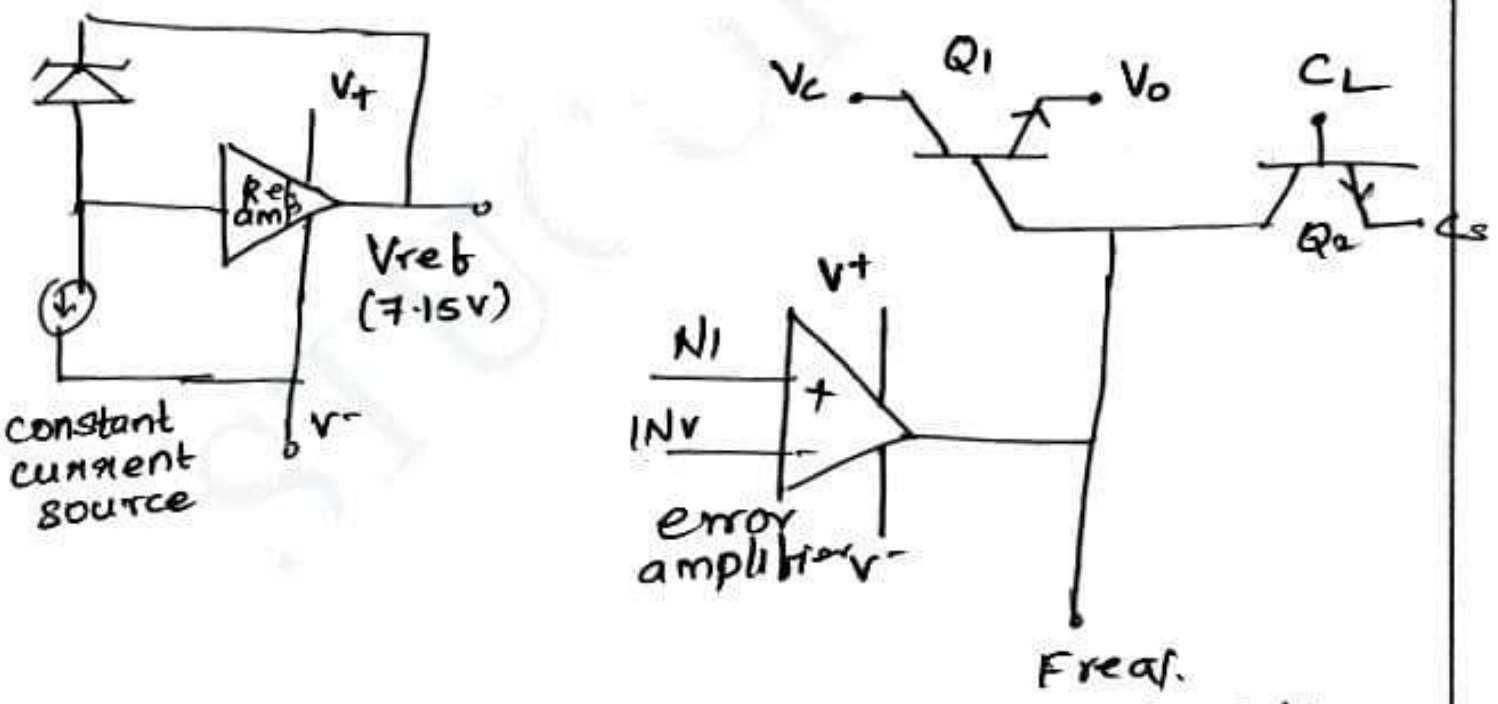
= 56.8 Hz

IC 723 GENERAL PURPOSE REGULATOR:

* In three terminal fixed voltage regulators have the following limitations.

1. No short circuit protection
2. output voltage is fixed

* The limitation have been overcome in the 723 general purpose regulators.
* The zener diode, a constant current source and reference amplifier produce a fixed voltage of about 7 Volts at the terminal Vref.
* The constant current source forces the zener to operate at a fixed point so that the zener output a fixed voltage.



* The power transistor Q_1 is in series with unregulated power supply V_{in} and regulated output voltage V_o.
* So it must absorb the difference between these two voltages whenever any fluctuation in output voltage V_o occurs.

* The transistor Q_1 is also connected as an emitter follower and therefore provides sufficient current gain to drive the load.

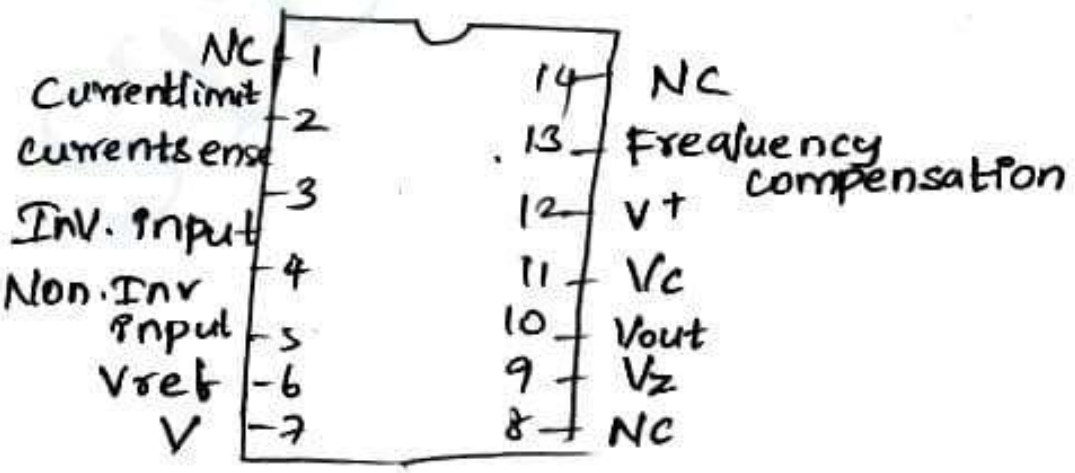
* The output voltage is sampled by R_1-R_2 divide and fed back to the (-) input terminal of the op-amp error amplifier.

* This sampled voltage is compared with the V_{ref}. The output V_o of the error amplifier drives the series transistor Q_1.

* If output voltage increases (i.e) due to variation in load current, the sampled voltage βV_o also increases.

$$\beta = \frac{R_2}{R_1 + R_2}$$

* In turn reduces output voltage V_o of differential amplifier due to 180° phase difference provided by op-amp V_o is applied to base of Q_1 which is used as an emitter follower



PIN DETAIL OF IC 723

A voltage regulator is an electronic circuit that provides a dc voltage independent of load current, temperature and ac line voltage

The circuit consist of 4 parts

1. Reference voltage circuit
2. Error amplifier
3. Series pass transistor
4. Feedback network

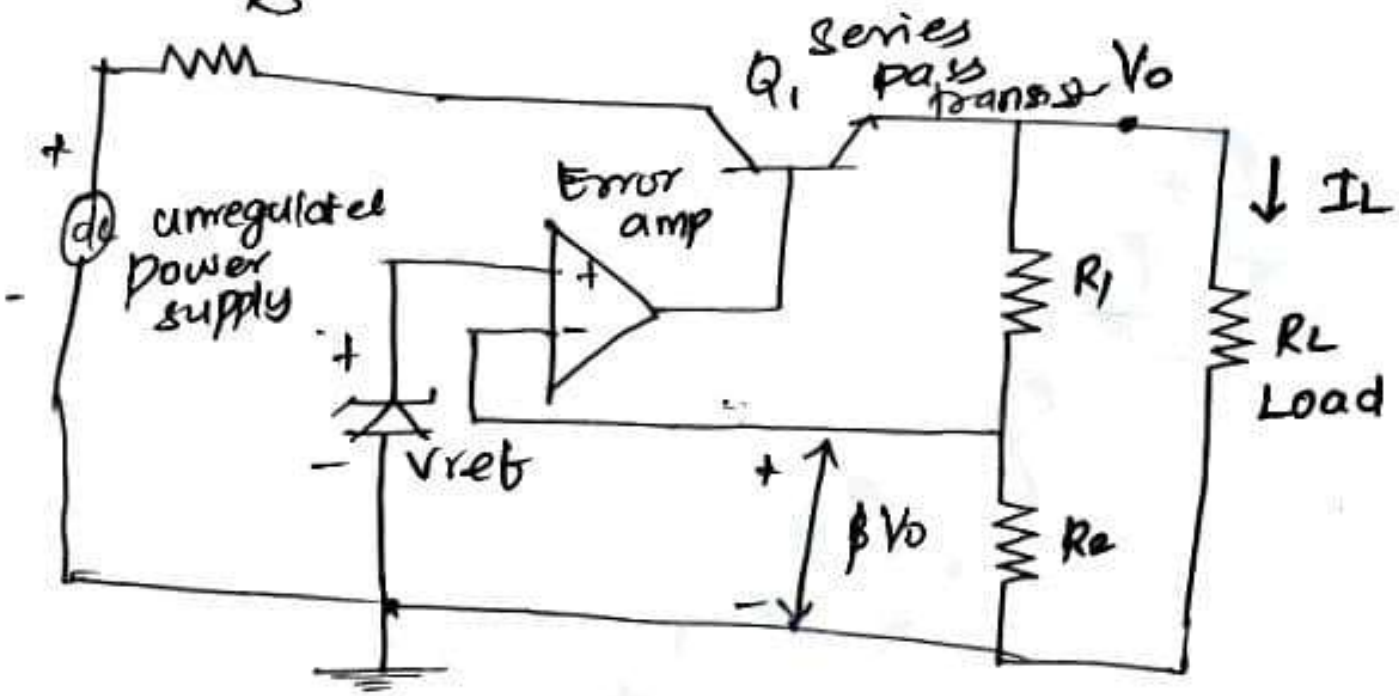
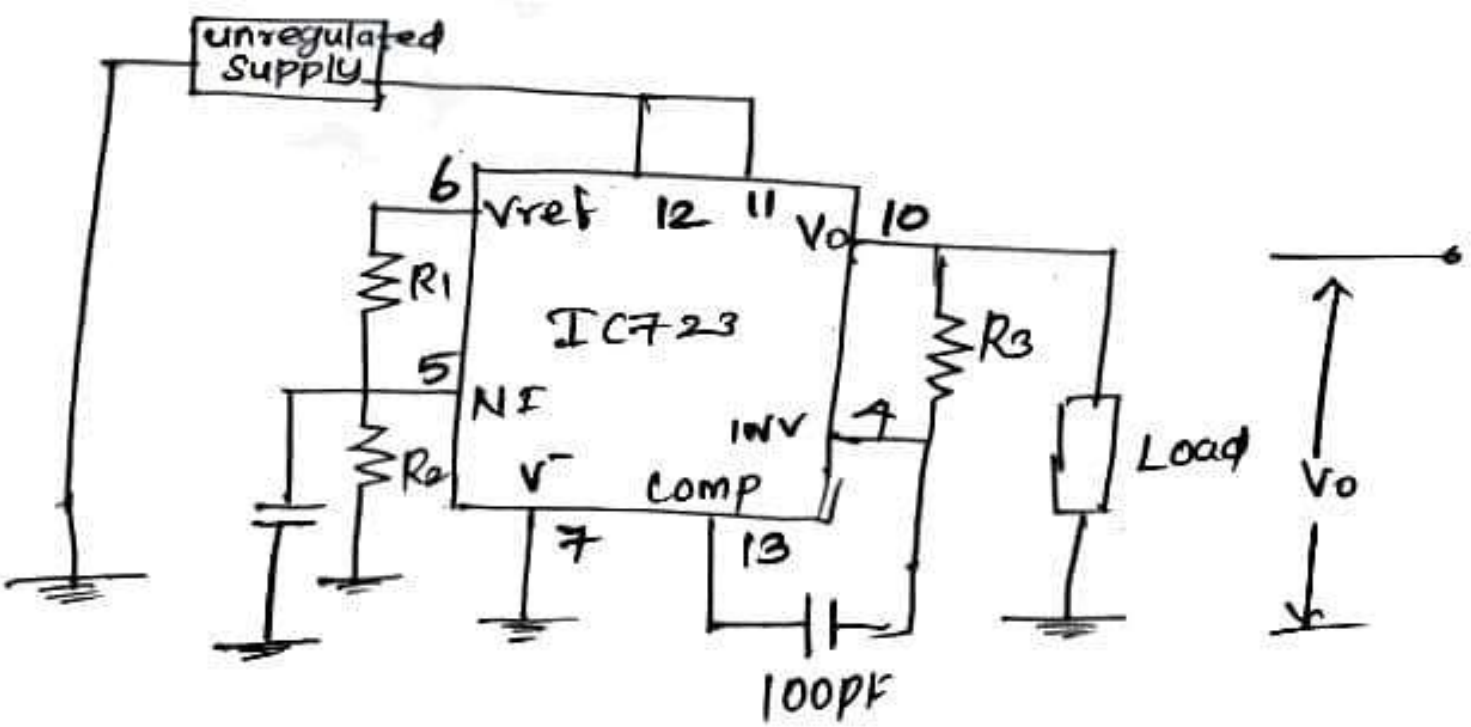


FIG: SERIES REGULATORS

MODES OF IC 723 REGULATOR



LOW POWER REGULATOR USING IC723

*A simple positive low voltage regulator (2v to 7V).

* The voltage at NI terminal of the error amplifier due to R_1 R_2 divider is

$$V_{NI} = V_{ref} = \frac{R_2}{R_1 + R_2}$$

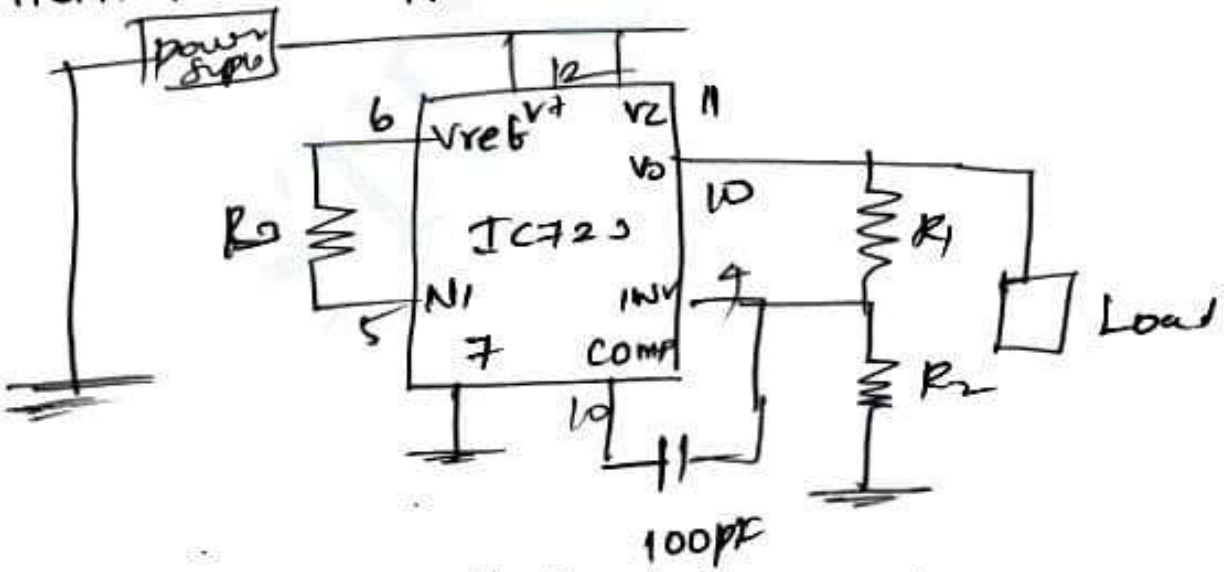
* The difference between V_{NI} and output voltage V_o which is directly fedback to the INV terminal is amplified by the error amplifier

$$V_o = V_{ref} \frac{R_2}{R_1 + R_2}$$

The reference voltage is typically 7.15 V. So the output voltage V_o is

$$V_o = 7.15 \times \frac{R_2}{R_1 + R_2}$$

HIGH VOLTAGE REGULATOR USING IC 723



* The circuit produce regulator output voltage greater than 7V. The NI terminal connects directly to Vref through R_3.

$$A_V = 1 + \frac{R_1}{R_2}$$

$$V_o = V_{ref}\left(1 + \frac{R_1}{R_2}\right)$$

$$V_o = 7.15\left(1 + \frac{R_1}{R_2}\right)$$

AUDIO POWER AMPLIFIER:-

* The amplifier receives an input from a signal source or from a transducer and gives out an amplified signal to the output device.

* Small signal amplifiers are generally voltage amplifiers.

Feautures of an Audio power Amplifier:-

(i) low power audio amplifier - 0 to 50 mW

(ii) Medium power audio amplifier - 50 mW to 500 mW

(iii) High power audio power amplifier - More than 500 MW

The design of heat sink for the Ic determines the amount of power deliverable by an amplifier.

The power conversion Efficiency of the amplifier is defined as $\eta = \frac{Pac}{Pdc}$ where Pac is the ac output power at the load and pdc is the dc input supplied to the Amplifier by the dc input supply.

Classification and operation of power Amplifiers:-

The operating point of the transistor circuit is fixed by selecting proper biasing

Based on the position of the Q-point on the load line, some classifications of the power amplifiers are,

(i) Class A power Amplifier
(ii) Class B Power Amplifier
(iii) Class AB power Amplifier

LM380 Audio power Amplifier:-

Feautures:-

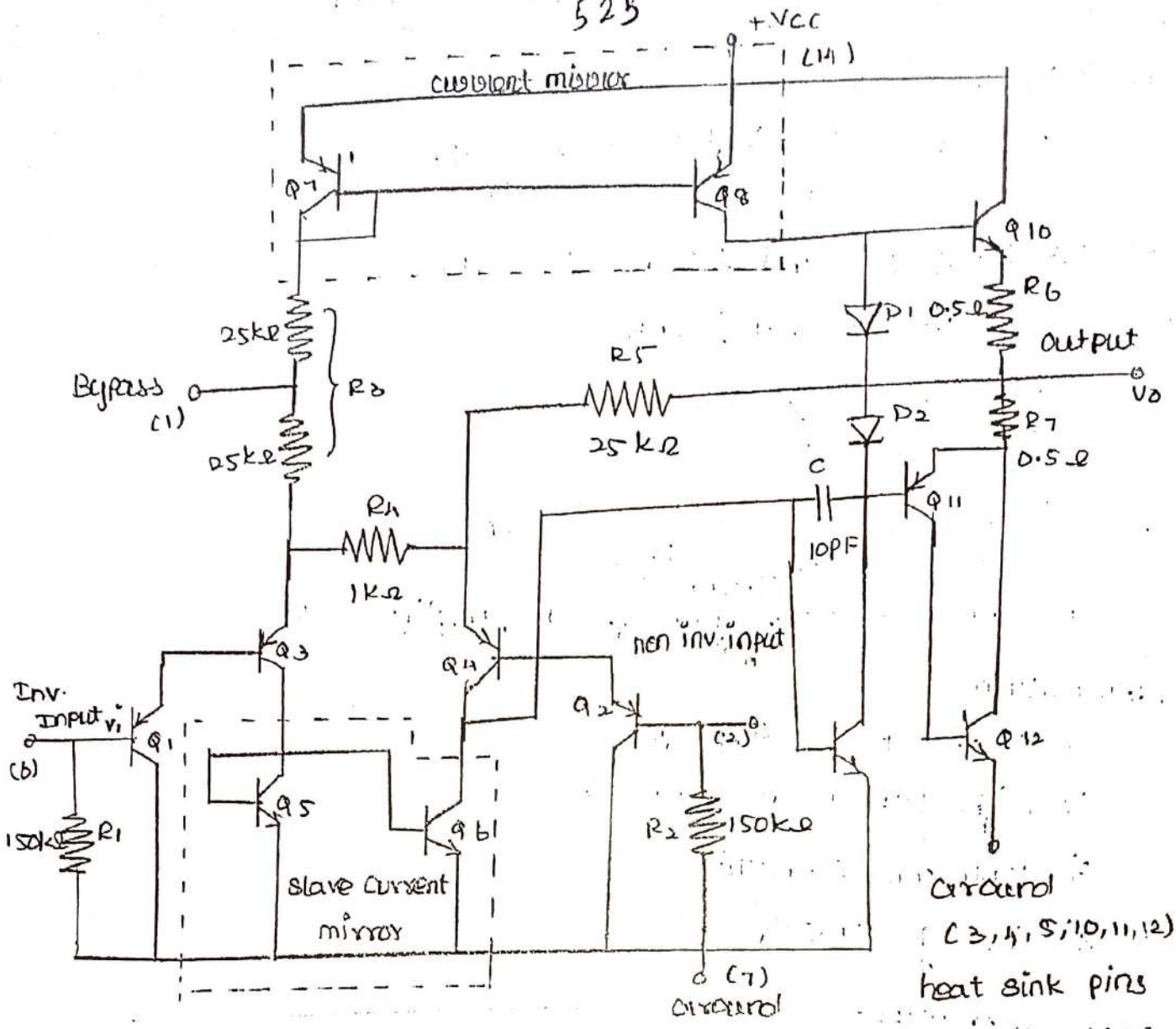
1) It operates with low quiescent power drain
2) It has low distortion
3) It can operate at temperature of 0°C to 70°C
4) It can delivered high peak current of 1.3 A Maximum.
5) Voltage gain of 34dB can be achieved.

CIRCUIT DISCRIPTION OF LM380:-

It consists of four stages, namely

(i) PNP Emitter follower
(ii) Differential amplifier
(iii) Common emitter Amplifier and
(iv) Quasi - complementary emitter follower.

* The Transistor Q1 and Q2 is PNP emitter follower input stage.
* Its output drives the Q3-Q4 PNP differential pair.
* The Q5 and Q6 act as collector loads for Q3 - Q4.
* Q7 and Q8 establishes the collector current of Q9.
* Q9 forms the common - emitter amplifier stage.
* D1, D2 & Q8 act as an active current source load.



The capacitor C is connected to Q9 to provide Internal compensation.

This enables upper cutt off frequency of 100 KHz at 2W for 8 loads.

The output stage is a Quasi - complementary pair emitter follower stage.

A dc feedback is introduced to the emitter of Q4 through Resistor R5.

This stabilises the output.

$$I_3 = \frac{V - V_{EB7} - V_{EB3} - V_{EB1}}{R_3} \simeq \frac{V - 3V_{EB}}{R_3}$$

I_4 of Transistor Q_4

$$I_4 = \frac{V_o - V_{EB4} - V_{EB2}}{R_5} \simeq \frac{V_o - 2V_{EB}}{R_5}$$

equate I_3 & I_4 and Assume $R_3 = 2R_5$.

$$V_o = \frac{1}{2}V + \frac{1}{2}V_{EB}$$

$$\frac{V_i}{R_4} + \frac{V_o}{R_5} + \frac{V_i}{R_4} = 0.$$

$$\therefore \frac{V_o}{V_i} = 2\frac{R_5}{R_4} = -2\frac{25\times10^3}{1\times10^3} = -50.$$

Thus the overall Internal gain of the amplifier is 50.

Applications:-

1) Audio power Amplifier
2) High gain audio amplifier
3) Intercom connections
4) Bridge amplifier.

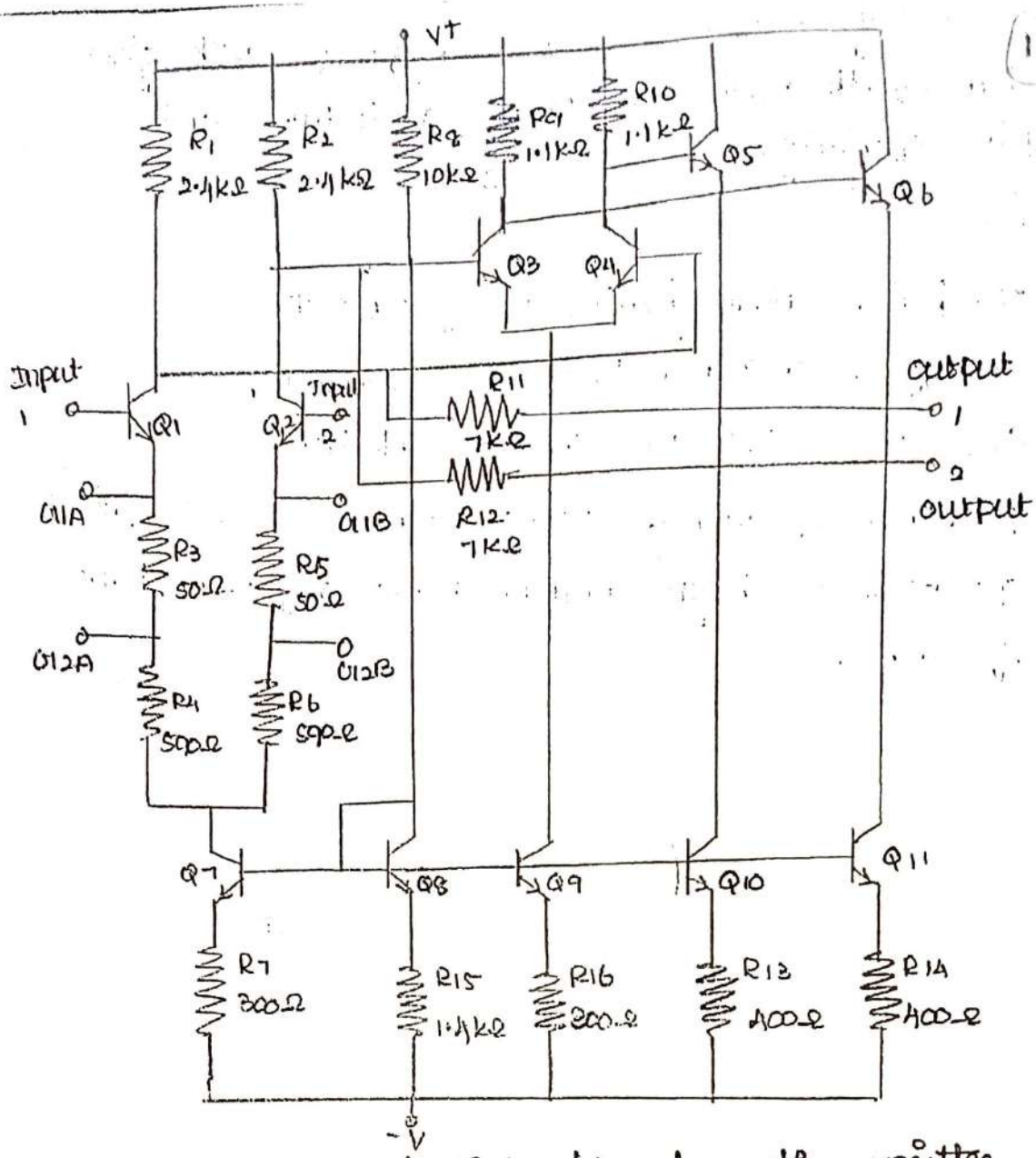
VIDEO AMPLIFIER:-

* The Vedio or wideband amplifiers are designed to provide a relatively flat gain versus frequency Response Characteristics for the range of Frequencies required to Transmit Video Information.

* The frequency Range 2dHz to several MHz
* The Tv required Bandwidth of 4 to 6 MHz
* The op-amp is normally operated in a closed loop configuration

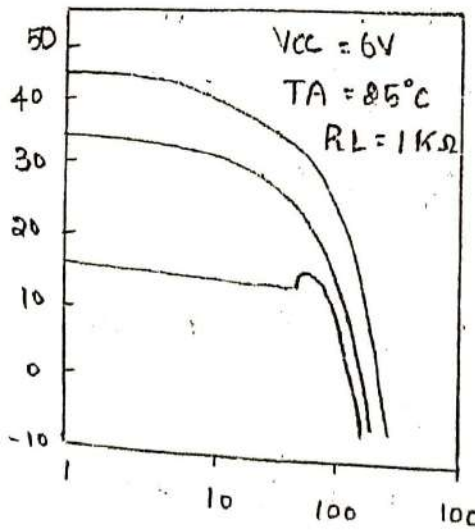
TYPE 733 VEDIO AMPLIFIER

It is a two - stage, differential Input,



* Q10 & Q11 act as current sink bias for the emitter Followers.

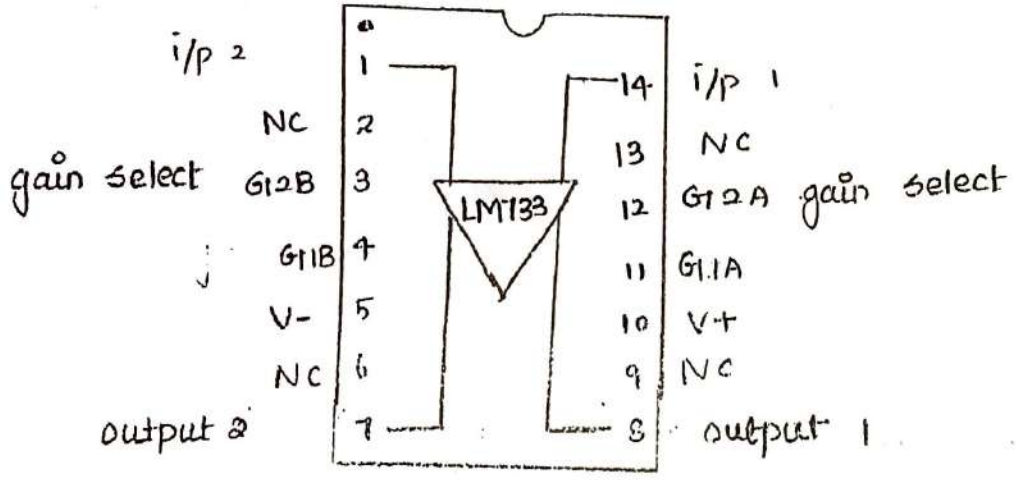
* The Resistor R11 & R12 provide negative feedback from the output terminals to balance i/p Terminals.



The use of Internal series - shunt feedback gives Wide bandwidth with low phase distortion and High gain stability.

Feautures :-

* It has a wide bandwidth of 120 MHz
* It offers an Input Resistance of 250 kΩ
* Gain of 10, 100 and 400 are selectable
* External frequency compensation is not Required
* It provides high common mode rejection Ratio at high frequencies.



Internal circuit diagram and operation :-

* The Internal circuit diagram of Type T33 monolithic Video amplifier.

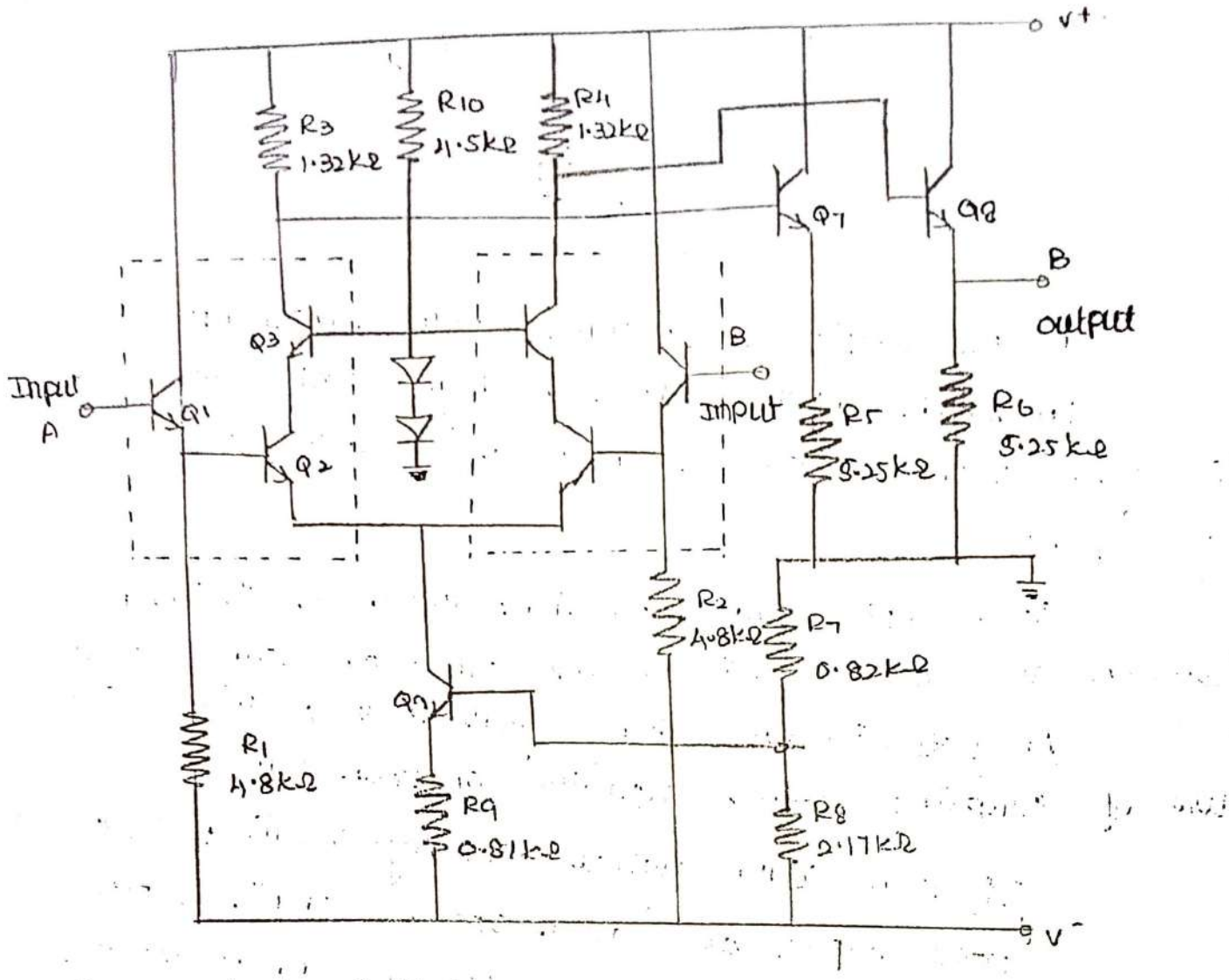
* It consists of two cascaded BJT differential amplifiers and a balanced emitter follower stage.

* The Input stage consists of Q1, Q2 and load Resistance R_1 and R_8.

* Resistor R3 Through R6 provide the negative Feedback path within the first stage.

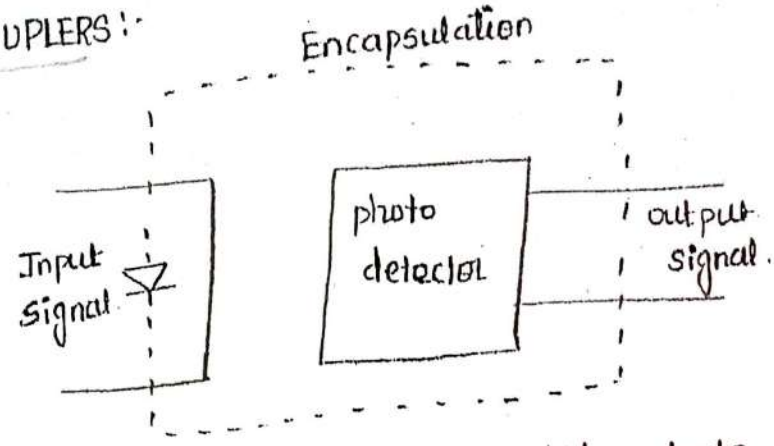
* Resistor R9 & R_{10} act as load Resistors.

TYPE 3040 Video Amplifier :-



The monolithic video amplifier IC 3040 from RCA uses a differential cascode configuration in the input stage. The input stage is formed by CC/CE compound connection of transistors Q_1, Q_2 and Q_3 operated in CE, CC and CB configuration respectively Q_4, Q_5, Q_6 are connected to a symmetrical configuration. Q_7, Q_8 provide a low impedance differential output from the circuit. Q_9 provide current sink biasing for the differential circuit. R_3 and R_4 act as load resistor. The R_5 and R_6 bias the emitter followers transistor Q_7 and Q_8. The diodes D_1 and D_2 with the resistor R_{10} provide a dc bias voltage for the transistor Q_2, Q_3, Q_5 and Q_6. The Q_9 is applied by the voltage divider using the resistor R_7 and R_8.

OPTO COUPLERS:



An opto coupler is a solid state component. In which light emitter, the light path and the light detector are all enclosed within the component

As the opto-coupler provides electrical isolation between two circuits, it is also called an opto-isolator.

An opto-isolator allows signal transfer without the use of coupling wires, capacitors or transformers

It can couple digital or analog circuits for signals.

opto coupler also called opto-electronic coupler.

It consists of Infrared LED and photo detector

The opto isolator Transduce a light Intensity by using LEDs.

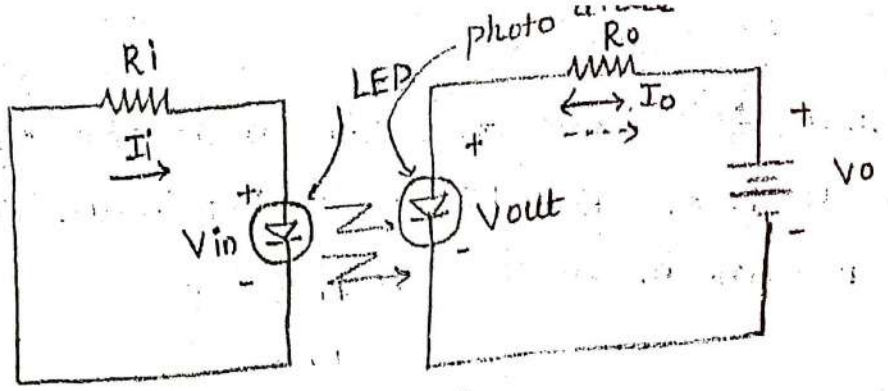
GaAs used to spectral matching with the silicon sensors.

It varies with temperature -55 to +55°C.

The switching time of opto-isolator decreases with increased current.

The light emitted from LED depends on the signal Vi.

Ro proportional to input voltage



Characteristics of opto-couplers:-

Collector-emitter voltage:-

Maximum voltage that can be applied across collector and emitter receiving phototransistors before it may break down.

Creepage distance:-

It is physical Measure. If the packages contaminate on it solder flux, or dampness will be created for noise signal to travel along the surface.

Forward current:-

This is the current passing through the trasmitting LED.

Forward voltage:-

Voltage that is drop across LED when it is turn ON by the Input signal Vi.

Collector dark current:-

current that can flow through the output photo Transistor when it is turned OFF.

collector-Emitter saturation voltage:-

Voltage available between the collector and emitter when transistor in O/p is turn ON

Isolation Resistance:-

This is the Resistance from a pin on the Input side to the output side.

Response time:-

The Rise and fall times duration that the o/p voltage requires to rise from zero to Maximum and to fall from maximum to zero respectively

cutt off frequency:-

This is effectively the highest frequency of Square-wave that can be applied to the opto-isolator

current Transfer Ratio:-

The input current is the forward current of LED that generates the emission of light, which is detected by photo diode, photo Darlington or photo SCR to produce the output current. The ratio of output current Io to the input current Ii is called the current Transfer Ratio.

OPTO-coupler Ics:-

The opto-coupler Ics are available in a variety of packages.

It is six-pin mini DIP.

OPTO coupler:-

The Type TLP112 from Toshiba is a mini-flat coupler, suitable for surface mount assembly.

It consists of

(i) GaAlAs light emitting diode
(ii) high speed detector
(iii) single chip photodiode-Transistor.

Features:-

(i) An isolation voltage of 2500 V rms can be achieved
(ii) Switching speeds of $t_{PHL} = 0.8\ \mu s$, $t_{PLH} = 2\mu s$(max) is possible.
(iii) It is TTL compatible.

MOC3009 - MOC3012 series opto-couplers :-

* It consists of Gallium Arsenide - Diode Infrared source.
* Optically coupled Silicon Triac driver.

APPLICATIONS:-

* Solenoid / Valve controls
* Lamp ballasts
* Interfacing microprocessors
* Motor controls
* Incandescent lamp dimmers.

TLP141G opto-coupler:-

→ It is suitable for surface mount assembly.
→ It consists of photo-Thyristor

Features :-

(i) peak off-state voltage : 400 V (min)
(ii) Trigger LED current : 10 mA (Max)
(iii) on-state current : 150 mA (max) and
(iv) Isolation voltage : 2500 Vrms (min).

Applications :-

* Programmable Controllers
* Output Module
* Solid state relay

2) They are compact and portable

3) Easy Interfacing with logic devices is possible

4) They are more efficient than isolation Transformers and relays

5) The problems such as noise, transients and contact bounce etc.. are completely eliminated.

ISOLATION AMPLIFIER:

The isolation amplifier is an amplifier in which there is no physical contact between the input and output sections. These amplifier are used in applications requiring large common mode voltage difference between the input and the output sections. several thousands volts can exists between the two sections.

They used in medical instrumentation applications where the patients must be isolated and protected from the leakage currents. They are hybrid ICs and consists of an input amplifiers, a GaAs light emitting diode (LED), a silicon photo diode and an output amplifier

It is linearity of input - output characteristics. Typical isolation amplifier chips are 1S0100, 3450 - 3455 series from Burr Brown and AD293 and AD294 from Analog devices

IC ISO100 ISOLATION AMPLIFIER:

The IC ISO100 is an optically coupled isolation amplifier. It offers high accuracy, linearity and good stability against time and temperature. It needs careful directional matching of optical components.

The main features of the isolation amplifier ISO100 are as follows:

Supply voltage : ±18V

Isolation voltage : ac peak or dc 750 V

Input current : ± 1 mA

storage temperature range : $-40^{\circ}C$ to $100^{\circ}C$

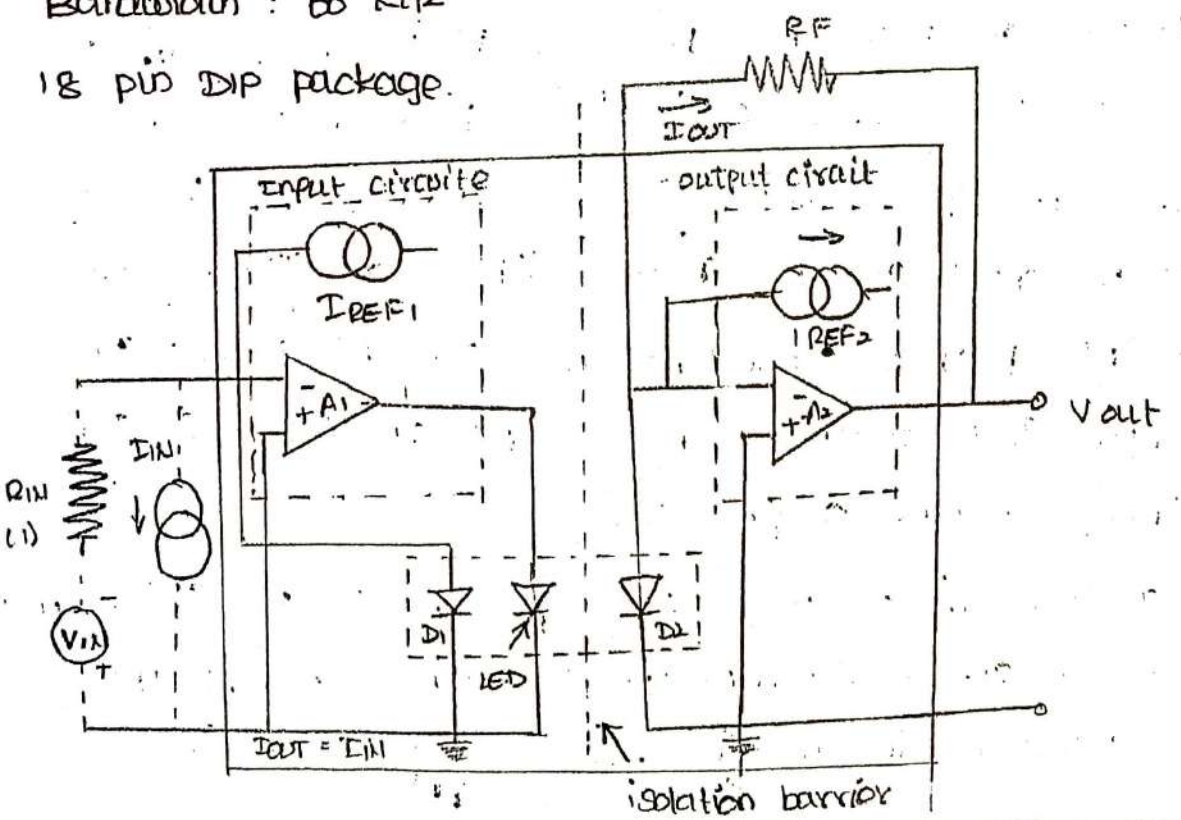
soldering lead temperature : $+300^{\circ}C$

output short circuit duration : continuous to ground

Leakage : 0.3 μA (max) at 240V / 60 Hz

Bandwidth : 60 KHz

18 pin DIP package.



The ISO100 has several modes of operations namely Unipolar or bipolar, voltage or current input and inverting or non inverting. It can be considered as high unity gain current amplifier. It output flows into a current to voltage converter. The isolation barrier exists between the input and output. The current at input device is replicated as I_{OUT} at output side of the device. The I_{OUT} is forced to flow through R_F. The non-inverting input of the IC ISO100 to the inverting input of op-amp A_1.

The transfer function of the IC ISO100 is given by $\frac{V_{OUT}}{V_{IN}} = \frac{R_F}{1+A_{GE}}$ where A_{GE} is the gain error.

It is defined as the deviation of the ratio, $\frac{I_{IN}}{I_{OUT}}$ from unity. It can thus be considered as the coupling error.

It consists of a matched pair of photo diodes and LED. The diode D_1 forms negative feedback path in LED. The diode D_2 receives the optical signal across the isolation barrier. The two matched current sources I_{REF_1} and I_{REF_2} are used for this purpose. connecting the current sources I_{REF_1} on the input side of the couplers and an equal current source I_{REF_2} on the output side.

The dc Error model used to represent ISO100. The element I_{OS} is called offset current. It is defined as the input current required for making the output voltage zero.

In unipolar operation, Ios are mismatch. In bipolar operation the mismatch between I_{REF_1} and I_{REF_2}. Ios is sensitive to temperature, supply voltage; common mode voltage and iso mode voltage. I_{D_1} and I_{D_2} represents the current generated by the photo diode D_1 and D_2 respectively.

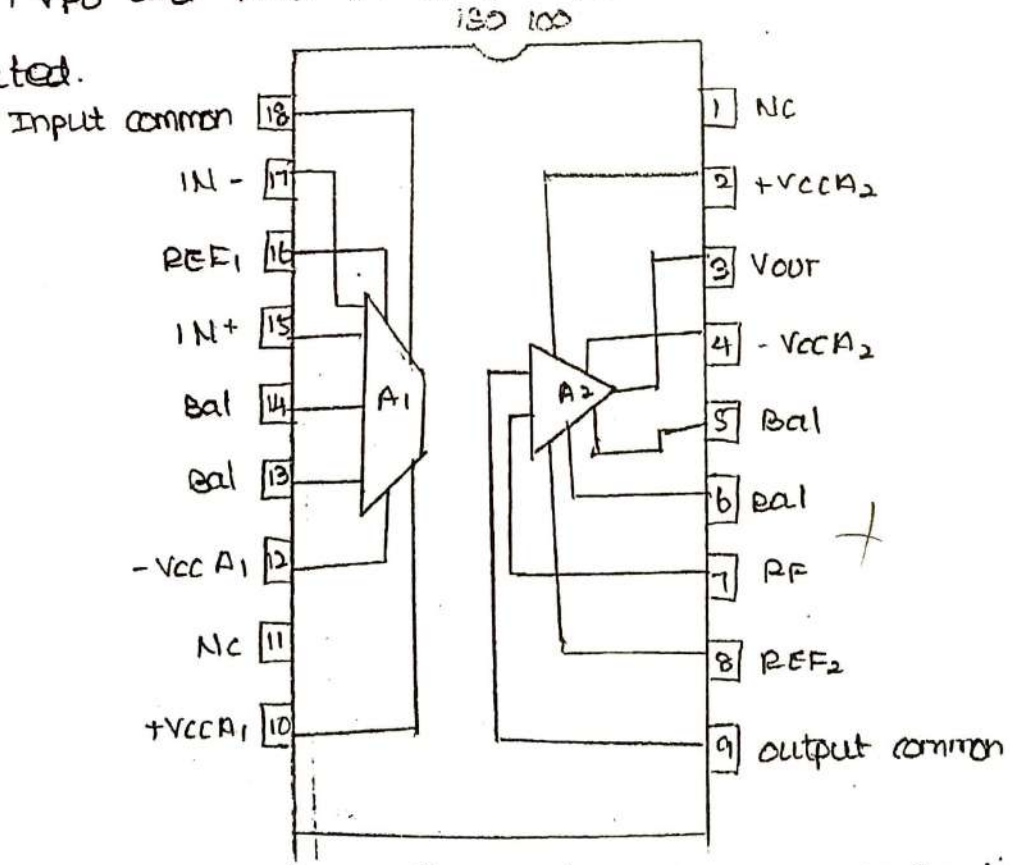
The two currents I_{D_1} and I_{D_2} are related as $I_{D_2} = I_{D_1}(1+A_{DIE})$. The tranfer function for the voltage mode is

$$V_O = R_F \left[\left(\frac{V_{IN}}{R_{IN}} + \frac{V_{OS1}}{R_{IN}} - I_{REF_1} + I_{OS} \right)(1+A_{DIE}) + I_{REF_2} \right] + V_{OSO}$$

The tranfer function for the input current is

$$V_O = R_F \left[I_{IN} - I_{REF_1} + I_{OS} \right](1+A_E)$$

It is noted that the power supply connections V_{P_1}, V_{N_1}, V_{PO} and V_{NO} to the input and output stages are isolated.



Pin configuration of ISO100 iso amplifier

Applications:

The advantages of ISO 100 are its small size, low offset low drift, wide bandwidth, ultra low leakage and low leakages.

The precautions are observed are as follows:

* Input common and IN lines at pins 17 and 18 must be grounded through seperate lines. This is to avoid any large dc current flowing in input common feedback to signal input.

* The external capacitance across the isolation barrier is to be minimised.