EC 8691 - MICROPROCESSOR AND MICROCONTROLLER (MCQ QUESTIONS WITH ANSWERS)

UNIT 1 and UNIT 2

8086 MICROPROCESSOR

1. If [CS]=348AH, [IP]=4214H, then the 20-bit physical address from which the code is accessed will be

(A) 455CAH (B) 0769EH (C) 390B4H (D) 38AB4H

Answer: D

Detailed Solution: Effective address= Base address of CS register X 10H + Address of IP

= 348AH X 10H + 4214H

= 38AB4H

2. Setting of direction flag in 8086 causes,

(A) The microprocessor to operate in single stepping mode

(B) The microprocessor to operate in break point mode

(C) The microprocessor string operations in auto increment mode

(D) The microprocessor string operations in auto decrement mode

Answer: D

Detailed Solution: If directional flag is set (1), then the string data is accessed from higher memory location towards lower memory location.

3. In order to read a word from the memory location 5000AH in a single bus cycle, the status of the 8086 signals A0 and BHE' should be

(A) A0 = 0, BHE', = 0

(B) A0 = 0, BHE' =1

(C) A0 = 1, BHE'= 0

(D) A0 = 1, BHE' = 1

Answer: A

Detailed Solution: As a word is to be read from the memory, $\overline{BHE}$ = 0 is used as a memory enable signal and the memory location 5000AH is even, A0 = 0 for even address.

4: If [BX]=0050H, [DS]=2000H, [00500H]=80H, [20050H]=08H, [CX]=5000H, then after MOV CL,[BX] instruction is executed the contents of CX will be

(A)0050H

(B)5008H

(C) 5080H

(D) 0008H

Answer: B

Detailed Solution: [DS] X 10H + [BX]

= 20000H + 0050H

= 20050H

After the execution of MOV CL,[BX] which copies the contents of the memory at address BX to CL, the contents of CX will be 5008H.

5: Before the execution of POP instruction the stack pointer points to FFFFH. The contents of the stack pointer after execution of POP instruction will be
(A) FFFFH (B) 0000H (C) 0001H (D) 0002H
Answer: C
Detailed Solution: After the execution of POP instruction, the stack pointer is automatically incremented by 2 to point to the next word on the stack.

6: If [AL]=35H and [BL]=39H, after the execution of the following instructions
ADD AL, BL
AAA
the contents of AL will be
(A) 6EH
(B) 3EH
(C) 14H
(D) 04H
Answer: D
Detailed Solution: Numerical data coming into a computer from a terminal is usually in ASCII code. In this code, the numbers 0 to 9 are represented by the ASCII codes 30H to 39H. The 8086 allows to add the ASCII codes for two decimal digits without masking off the "3" in the upper nibble of each. After the addition, the AAA instruction is used to make sure the result is the correct unpacked BCD. If the addition produces a decimal carry (AF=1), the AH register is incremented and the carry (CF) and auxiliary carry (AF) flags are set to 1. If the addition did not produce a decimal carry, CF and AF are cleared to 0 and AH is not altered. In both cases, the high-order 4 bits of AL are cleared to 0.

7: Which of the following is unpacked BCD number
(A) 23 (B) 2B (C) 08 (D) 0A
Answer: C
Detailed Solution: Unpacked BCD number contains only one decimal digit per byte. The digit is stored in the least significant 4 bits and rest of the bits are 0.

8: The WAIT instruction causes the 8086 to enter into ideal state until
(A) The LOCK' pin is made LOW
(B) The LOCK' pin is made HIGH
(C) The TEST' pin is made LOW
(D) The TEST' pin is made HIGH
Answer: C
Detailed Solution: If the TEST pin is Low, execution continues otherwise the processor waits in an "idle" state.

9: If [AX]=009BH, after the execution of CBW instruction the contents of AX will be
(A) 009BH (B) FF9BH (C) 0000H (D) 9B9BH
Answer: B

Detailed Solution: CBW converts the signed value in the AL register into an equivalent 16 bit signed value in the AX register by duplicating the sign bit to the left. This instruction copies the sign (bit 7) in the source operand into every bit in the AH register.

10: Which of the following is not an 8086 maximum mode signal?
(A) LOCK
(B) S0
(C)ALE
(D) QS0
Answer: C
Detailed Solution: ALE is a minimum mode signal.

11: What is the maximum capacity of the memory that can be interfaced to the microprocessor which contains 20 address lines?
a.) 64 KB
b.) 1 MB
c.) 64 MB
d.) 1 GB
Answer: B
Detailed Solution: Maximum Capacity = 2^{20} = 1048576 = 1MB

12: The size of ALU in 8086 is
a.) 8 bit
b.) 16 bit
c.) 24 bit
d.) 32 bit
Answer: B

13: Which of the following is used to sequence the execution of instructions
a.) Segment register
b.) Stack pointer
c.) Instruction pointer
d.) Flag register
Answer: C

14: What are the status of carry and auxiliary carry flags after performing the subtraction of 0FH from F0H
a.) Both the flags are reset
b.) Both the flags are set
c.) Carry flag is set and auxiliary carry flag is reset
d.) Carry flag is reset and auxiliary carry flag is set
Answer: D

Detailed Solution: Consider the Subtraction as follows:

Since Minuend is greater than Subtrahend, there will be no carry. Hence the Carry flag will be reset. In this arithmetic operation, a borrow is transferred from bit position 4 to bit position 3. Hence auxiliary carry flag will be set.

15: If [CS] = 5500H, [IP] = 1200H, then the 20-bit physical address would be
a.) 56200H b.) 67000H c.) 17500H d.) 57500H

Answer: A
Detailed Solution: Effective Address = Base address of CS register × 10H + Address of IP
= 5500H × 10H + 1200H = 56200H

16: The 8086 XLAT is used to
a.) Exchange the contents of memory with register b.) Convert the byte into word
c.) Convert the word into double word d.) Convert the ASCII into EBCDIC
Answer: D

17: What is the ASCII code corresponds to decimal 9
a.) 39H
b.) 49H
c.) E9H
d.) F9H

Answer: A

18: In order to perform multi-byte addition, which of the following instruction will be used
a.) ADD
b.) ADC
c.) AAA
d.) AAD
Answer: B

19: What will be the contents of AX after execution of the following instructions
MOV AL, FFH
MOV BL, 05H
MUL BL

a.) 04FAH b.) 04FBH c.) 04FCH d.) 04FDH
Answer: B
Detailed Solution: After execution of 1st instruction, the content of AL is FFH i.e 255 in decimal. Similarly, after execution of 2nd instruction, the content of BL is 05H i.e 05 in decimal. The third instruction multiplies content of BL (05) with that of AL (i.e) 255 and stores the result in AX. We know that 255 × 5 = 1275 which is equal to 04FBH in hexadecimal.

20: What will be the contents of AL after execution of the following instructions
MOV AL, 65H

MOV BL, 75H
ADD AL, BL
DAA

a.) DAH
b.) E0H
c.) 40H
d.) 41H
Answer: C
Detailed Solution: Upon the execution of 1st and 2nd instruction, we have 65H and 75H in AL and BL respectively. The third instruction adds the content of AL and BL and the result is stored in AL. Consider the following:
0110 0101 (65H) + 0111 0101 (75H) = 1101 1010 (DAH)

Now, the DAA instruction adds 0110 (6H) to first nibble i.e 1010, if greater than 1001 (9H). Similarly, it adds 0110 (6H) to second nibble i.e. 1101, as well because it is also greater than 1001 (9H). As a result, we get the final result as, 1101 1010 + 0110 0110 = 0100 0000 (40H).

21: What will be the contents of AL after execution of the following instructions
MOV AL, 39H
MOV BL, 34H
ADD AL, BL
AAA
a.) 6DH
b.) 13H
c.) 33H
d.) 03H
Answer: D
Detailed Solution: https://www.youtube.com/watch?v=-z1U-ys8HCc

22: If [DL]=EFH and carry flag is reset, what will be the contents of DL after execution of the instruction ROL DL,01H
a.) 5FH
b.) DFH
c.) F7H
d.) 77H
Answer: B
Detailed Solution: The instruction, ROL DL,01H, rotates the content of [DL] by one bit to the left. The content of DL is EFH which is 1110 1111 in binary. When we rotate it by 1 bit to the left we get 1101 1111 which is DFH in hexadecimal.

23: If [AL]=EFH, after the execution of NEG AL, the contents of AL would be
a.) 00H
b.) 10H
c.) 11H

d.) 12H
Answer: C
Detailed Solution: EFH is equal to 1110 1111 in binary. The NEG AL instruction corresponds to 2's complement of the content of AL which is 1110 1111. The 2's complement of 1110 1111 is 0001 0001 which is equal to 11H.

24: Which of the following instruction is equivalent to XOR AL, AL
a.) OR AL,00H
b.) AND AL,00H
c.) OR AL, FFH
d.) AND AL, FFH
Answer: B
Detailed Solution: Ex-OR of a quantity with itself is always 0. Also, when we do the AND operation of any quantity with 0, the result is always 0. Hence option B is the Answer.

25: After the execution of CALL instruction
(A) The contents of stack pointer will be incremented by 1
(B) The contents of stack pointer will be decremented by 1
(C) The contents of stack pointer will be incremented by 2
(D) The contents of stack pointer will be decremented by 2

Answer: D

26: The instruction REPZ CMPSB compares string bytes
(A) Until end of the string or until string bytes not equal
(B) Until end of the string or until string bytes equal
(C) Until end of the string or until string words not equal
(D) Until end of the string or until string words equal

Answer: A

27: Type 3 interrupt is
(A) Divide by zero interrupt
(B) Single step interrupt
(C) Breakpoint interrupt
(D) Interrupt on overflow
Answer: C
Detailed Solution: The starting address for type0 interrupt is 000000H, for type1 interrupt is 00004H similarly for type2 is 00008H and so on. The first five pointers are dedicated interrupt pointers. i.e. −

- TYPE 0 interrupt represents division by zero situation.
- TYPE 1 interrupt represents single-step execution during the debugging of a program.
- TYPE 2 interrupt represents non-maskable NMI interrupt.
- TYPE 3 interrupt represents break-point interrupt.
- TYPE 4 interrupt represents overflow interrupt.

The interrupts from Type 5 to Type 31 are reserved for other advanced microprocessors, and interrupts from 32 to Type 255 are available for hardware and software interrupts.

28: The size of interrupt pointer table in 8086 is
(A) 256 bytes
(B) 512 bytes
(C) 1024 bytes
(D) 2048 bytes
Answer: C

Detailed Solution: The interrupt vector table in the 8086/8088 is the first 1024 bytes in memory. There are 256 vectors, each containing 4 bytes, CS: IP, for each possible interrupt source.

29: After the execution of INT 2 instruction
A) The contents of stack pointer will be incremented by 2
(B) The contents of stack pointer will be decremented by 2
(C) The contents of stack pointer will be incremented by 4
(D) The contents of stack pointer will be decremented by 4

Answer: D
Detailed Solution: 8086 responds to the interrupt by performing series of actions:
1. It decrements stack pointer by 2 and pushes the flag register on the stack.
2. It disables the INTR interrupt input by clearing the interrupt flag in the flag
3. It resets the trap flag in the flag register.
4. It decrements stack pointer by 2 and pushes the current code segment register contents on the stack.
5. It decrements stack pointer by 2 and pushes the current instruction pointer contents on the stack.
6. It does an indirect far jump at the start of the procedure by loading the CS and IP values for the start of the interrupt service routine (ISR).

30: Which of the following instruction is used to pass the instructions from 8086 to coprocessor 8087?
(A) INT 3
(B) JMP
(C) LOCK
(D) ESC
Answer: D

31: The execution of WAIT instruction causes 8086 to enter into ideal state until
(A) The $\overline{TEST}$ pin is made LOW
(B) The $\overline{TEST}$ pin is made HIGH

(C) The $\overline{LOCK}$ pin is made LOW

(D) The $\overline{LOCK}$ pin is made HIGH

Answer: A
Detailed Solution: The WAIT instruction monitors the BUSY and TEST pin of 8086 Microprocessor. If TEST=0, then Microprocessor executes WAIT instruction until TEST=1.

32: If [DX]=0000H and [AX]=F000H, after the execution of the instruction CWD, the contents of DX and AX respectively are

(A) 0000H and F000H
(B) F000H and 0000H
(C) FFFFH and F000H
(D) F000H and FFFFH

Answer: C
Detailed Solution: CWD instruction enlarges the sign bit of a word into AX register to all the bits of the DX register. This is used before a signed word in AX is to be divided through another signed word by using IDIV instructions. No flags are influenced.

33: To evaluate which of the following expressions subroutine concept is useful

(A) $X + Y^2$ (B) $X^2 + Y$ (C) $X + Y$ (D) $X^2 + Y^2$

Answer: D
Detailed Solution: In option (D), two multiplications are involved. So, subroutine concept is useful.

34: An 8× 4 ROM can be constructed using

(A) A 2× 4 decoder and four 4-input OR gates
(B) A 2× 4 decoder and four 8-input OR gates
(C) A 3× 8 decoder and four 4-input OR gates
(D) A 3× 8 decoder and four 8-input OR gates

Answer: D
Detailed Solution: A 2k x n ROM will have an internal k x 2k decoder and n 2k-input OR gates.

35: The number of basic cells in a 16 × 4 RAM are

(A) 4 (B) 16 (C) 64 (D) 128

Answer: C
Detailed Solution: It consists of 16 words of 4 bits each and has a total of 64 binary cells.

36: Which of the following statement is TRUE

(A) Both ROM and RAM are combinational circuits
(B) ROM is a combinational circuit and RAM is a sequential circuit
(C) ROM is a sequential circuit and RAM is a combinational circuit
(D) Both ROM and RAM are sequential circuits

Answer: B

37: Which of the following memory is volatile
(A) ROM
(B) PROM
(C) EPROM
(D) RAM
Answer: D
Detailed Solution: Data in RAM is not permanently written. When you power off your computer the data stored in RAM is deleted.

38: Upon RESET, the 8086 microprocessor starts the operations from the memory location
(A) 0000H
(B)0FFFFH
(C)FFFF0H
(D)FFFFH
Answer: C
Detailed Solution: The reset pin of 8086 and other processors will cause the CS: IP to point to FFFF:0000 which is the lowest 16 bytes of the memory. In that location there is a jump instruction to somewhere else in the memory space to initialize the processor.

39: If the starting address of 1KB memory is 00500H, then the ending address would be
(A) 008FFH
(B) 00CFFH (C) 01400H (D) 01500H
Answer: A
Detailed Solution: 00500 H when converted to decimal becomes 1280 and 1KB = 1024, so 1280+1024 = 2304. So the memory location will be 2303 converted to hex which is 08FF H.

40: If the chip select of 8KB RAM is

$\overline{CS} = \overline{(A13)(A14)(A15)(A16)(A17)(A18)(A19)}$. The address range of RAM would be
(A) 00000H-1FFFFH
(B) FC000H-FFFFFH
(C) FE000H-FFFFFH
(D) FF000H-FFFFFH

Answer: C
Detailed Solution: The address lines are 0 to 19. In hexadecimal this range is from 00000 H to FFFFF H values. This entire range is not addressable because of the chip select line connected to the address lines 13 to 19. The CS line is driven by an A13 to A19 have values 1111 1110 0000 0000 0000 H to 1111 1111 1111 1111 1111 H. The final address range, which in hexadecimal is FE000 H to FFFFF H.

41: In order to program Port A and Port B as output ports in Mode 0 and Port C as input port in Mode 0, the control word for 8255 would be

(A) 89H
(B) 98H
(C) 6FH
(D) F6H

Answer: A
Detailed Solution: https://www.geeksforgeeks.org/programmable-peripheral-interface-8255/

42 : The time taken to execute MOV CX, FFFFH using 8086 with 5 MHz clock would be

(A) 0.2 µs
(B) 0.4 µs
(C) 0.6 µs
(D) 0.8 µs

Answer: D
Detailed Solution: https://theencarta.com/mov-instruction-8086/

43: The number of clock cycles required to execute NOP operation of 8086 is

(A) 1
(B) 2
(C) 3
(D) 4

Answer: C
Detailed Solution: At the time of execution of NOP instruction, no operation is performed except fetch and decode. It takes three clock cycles to execute the instruction. NOP instruction does not affect any flag. This instruction is used to fill in time delays or to delete and insert instructions in the program while trouble shooting.

44. Number of the times the instruction sequence below will loop before coming out of loop is

```
MOV AL, 00h
A1: INC AL
JNZ A1
```

(A) 00
(B) 01
(C) 255
(D) 256
Ans Answer is (D)

45. What will be the contents of register AL after the following has been executed

```
MOV BL, 8C
```

MOV AL, 7E
ADD AL, BL
(A) 0A and carry flag is set (B) 0A and carry flag is reset
(C) 6A and carry flag is set (D) 6A and carry flag is reset
Ans, Result is 1,0A. Hence answer is (A).

46. Direction flag is used with
(A) String instructions. (B) Stack instructions.
(C) Arithmetic instructions. (D) Branch instructions.
Ans The direction flag is used only with the string instructions. Hence answer is (A).

47. Ready pin of a microprocessor is used
(A) to indicate that the microprocessor is ready to receive inputs.
(B) to indicate that the microprocessor is ready to receive outputs.
(C) to introduce wait states.
(D) to provide direct memory access.
Ans This input is controlled to insert wait states into the timing of the microprocessor.
Hence answer is (C).

48. These are two ways in which a microprocessor can come out of Halt state.
(A) When hold line is a logical 1.
(B) When interrupt occurs and the interrupt system has been enabled.
(C) When both (A) and (B) are true.
(D) When either (A) or (B) are true.
Ans Answer is (A)

49. LOCK prefix is used most often
(A) during normal execution. (B) during DMA accesses
(C) during interrupt servicing. (D) during memory accesses.
Ans LOCK is a prefix which is used to make an instruction of 8086 non-interruptable.
Hence answer is (C).

50. The Pentium microprocessor has_____execution units.
(A) 1
(B) 2
(C) 3
(D) 4
Ans The Pentium microprocessor is organized with three execution units. One executes floating-point instructions, and the other two (U-pipe and V-pipe) execute integer instructions. Hence answer is (C).

51. The memory data bus width in Pentium is
(A) 16 bit
(B) 32 bit

(C) 64 bit
(D) None of these
Ans The Data bus width is 64 bits. Hence answer is (C).

52. The no. of address lines required to address a memory of size 32 K is
(A) 15 lines (B) 16 lines
(C) 18 lines (D) 14 lines

Ans 32K= 32X1024bits= $2^5X2^{10}=2^{15}$. Hence answer is (A).

53. NMI input is
(A) Edge sensitive (B) Level sensitive
(C) Both edge and level triggered (D) edge triggered and level sensitive

Ans Non-maskable interrupt (NMI) is an edge –triggered input that requests an interrupt on the positive edge (0 to 1 transition).

54. How many types of basic multiprocessor configurations?
A. 2
B. 3
C. 4
D. 5
Ans : B

Explanation: Multiprocessor means a multiple set of processors that executes instructions simultaneously. There are three basic multiprocessor configurations : Coprocessor configuration, Closely coupled configuration and Loosely coupled configuration.

55. A _____ is a specially designed circuit on microprocessor chip which can perform the same task very quickly, which the microprocessor performs
A. Coprocessor configuration
B. Closely coupled configuration
C. Loosely coupled configuration
D. None of the above

Ans : A

56. The coprocessor and the processor is connected via?
A. TEST
B. QS0
C. QS1
D. All of the above

Ans : D

Explanation: The coprocessor and the processor is connected via TEST, RQ-/GT- and QS0 & QS1 signals.

57. _____signal takes care of the coprocessor's activity, i.e. the coprocessor is busy or idle.
A. TEST
B. QS0
C. QS1
D. None of the above
Ans : A

58. Which of the following are advantage of Loosely Coupled Configuration?
A. Having more than one processor results in increased efficiency.
B. easy to achieve parallel processing.
C. system structure is flexible
D. All of the above

Ans : D

59.. 8087 numeric data processor is also known as?
A. Math co-processor
B. Numeric processor extension
C. Floating point unit
D. All of the above

Ans : D

60. 8087 Architecture is divided into?
A. 2
B. 3
C. 4
D. 5

Ans : B

Explanation: 8087 Architecture is divided into two groups, i.e., Control Unit (CU) and Numeric Extension Unit (NEU).

61. The _____ handles all the communication between the processor and the memory
A. numeric extension unit
B. Packed Unit
C. control unit
D. Binary Unit

Ans : C

62. 8087 Numeric Data Processor designed by?
A. Intel
B. IBM
C. Microsoft
D. VAX

Ans : A

Explanation: It was the first math coprocessor designed by Intel to pair with 8086/8088 resulting in easier and faster calculation.

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(MCQ QUESTIONS WITH ANSWERS)

UNIT 3
I/O INTERFACING

1. Which of the following operation is not involved in interfacing a keyboard to 8086

(A) Detect a keypress
(B) Debounce the keypress
(C) Decode the keypress
(D) Encode the keypress
Correct Answer: C

2. The process of making sure a previous key has been released before looking for next one is called

(A) Decoding of the key
(B) Debouncing of the key
(C) Encoding of the key
(D) Two key lockout

Correct Answer: D

3. In order to interface a hexadecimal keyboard to 8086

(A) One 8-bit port of 8255 must be programmed as input port and 4-bits of another port must be programmed as output port
(B) One 8-bit port of 8255 must be programmed as output port and 4-bits of another port must be programmed as input port
(C) One 8-bit port of 8255 and 4-bits of another port must be programmed as output ports
(D) 01500H One 8-bit port of 8255 and 4-bits of another port must be programmed as input ports
Correct Answer: A

4. Let a BCD to 7-segment decoder (7447) is interfaced to a common anode type 7- segment display. If the BCD input to 7447 is 1001 and common signal of 7-segment display is connected to logic 1,
    a. All the segments of display will be at logic 0
    b. Only the segment “e” will be at logic 0
    c. All the segments except “e” will be at logic 0
    d. All the segments except “e” will be at logic 1

    Correct Answer: C

5. In order to rotate stepper motor in anti-clockwise direction, which of the following bit sequence need to be applied to its windings
    a. 0011,1001,1100,0110
    b. 0110,1100,1001,0011
    c. 1000,1100,1110,1111
    d. 1111,1110,1100,1000

    Correct Answer: B

6. In order to start the conversion, the WR signal of A/D converter 0804 must be

a. Kept HIGH
b. Kept LOW
c. Changed from LOW to HIGH
d. Changed from HIGH to LOW

Correct Answer: C

Detailed Solution: WR which is connected to PC3 of 8255, acts as start of conversion signal so whenever microprocessor wants to start any conversion, WR changed from LOW to HIGH.

7. The end of conversion of A/D converter 0804 is represented by
   a. INTR = 0
   b. INTR = 1
   c. WR = 0
   d. WR = 1

   Correct Answer: A

8. For $\pm$5V analog input voltage range, the A/D converter 0804 produces digital output in the range of 00H to FFH. If the input analog voltage is 0 V, the corresponding digital output would be
   a. 00H
   b. 70H
   c. 80H
   d. 90H

   Correct Answer: C

   Detailed Solution: Total range of voltage is +5 V to -5V, i.e., total voltage is 10V and the bit range is 8 bit (00H to FFH). So each step has a voltage of 10V/255(28-1)=0.039V. It is given that -5V is 00 H, so 0V, i.e., -5V+5V=0V, there is 5V difference between 0V and -5V. So 0.039 shows one step so 5V shows 5V/0.039 steps, i.e., 128 steps. So 0V will be represented by 00H (for -5V) +128=128=10000000=80H (for 0V).

9. For 0 – 5V analog input voltage range, the A/D converter 0804 produces digital output in therange of 00H to FFH. If the input analog voltage is 0.196 V, the corresponding digital output would be
   a. 01H
   b. 05H
   c. 0AH
   d. 10H

   Correct Answer: C

   Detailed Solution: Total range of voltage is 0 V to 5V, i.e., total voltage is 5V and the bit range is 8 bit (00H to FFH). So each step has a voltage of 5V/255(2^8-1) =0.0196V. It is given that 0V is 00 H, so 0.196V, i.e., 0V+0.196V=0.196V, there is 0.196V difference between 0V and 0.0196V. So 0.0196 shows one step so 0.196V shows 0.196V /0.0196 steps, i.e., 10 steps. So 0.196V will be represented by 00H (for 0V)+10=00001010=0AH (for 0.196V).

10. If 0800 would be
    a. 1 mA
    b. 2 mA

c. 3 mA
d. 4 mA

IREF = 2mA and digital input to D/A converter IC 0800 is 10000000, the output current of

Correct Answer: A
Detailed Solution: IOUT = IREF ((1/2) Bn+(1/4) Bn-1+…. +(1/2) n B0) = 2mA ((1/2) x1+0) =1mA

11. A 5 K Ω feedback resistor is connected in the current to voltage converter at the output of D/A converter. If the digital input to IC 0800 is FFH, the analog output voltage for bipolar operation would be
    a. -10 V
    b. 0 V
    c. +5 V
    d. +10 V

    Correct Answer: C and D

12. In the above question 7, the analog output voltage for unipolar operation would be
    a. -10 V
    b. 0 V
    c. +5 V
    d. +10 V

    Correct Answer: C and D

13. If the address of 8254 control word register is 97H, the address of counter 0 would be
    a. 96H
    b. 95H
    c. 94H
    d. 93H

    Correct Answer: C
    Detailed Solution: The least significant two bits are used to point counter 0, counter 1, counter 2 and Control word register. 00 for counter 0, 01 for counter 1, 10 for counter 2 and 11 for control word register. In this way, if 97H points to CWR then 96H would point to counter 2, 95H for counter 1 and 94H for counter 0.

14. If 0FH is loaded into control word register of 8254, then the mode selected would be
    a. Mode 2
    b. Mode 3
    c. Mode 4
    d. Mode 5

    Correct Answer: B
    Detailed Solution: 0FH corresponds to 0000 1111. So, M2, M1 and M0 is 111 which corresponds to Mode 3.

15. In mode 0 of 8254, the GATE input must
    a. kept LOW
    b. kept HIGH

c. change from LOW to HIGH
d. change from HIGH to LOW

Correct Answer: B

16. Which of the following mode generates square wave?
    a. Mode 2
    b. Mode 3
    c. Mode 4
    d. Mode 5

    Correct Answer: B

17. In order to read the count in the 8254 counter while count is still going on, which of the following operation would be performed?
    a. Latching
    b. Triggering
    c. Strobe
    d. Single stepping

    Correct Answer: A

18. If the chip select of 8254 is generated using , the address of counter 2 would be
    a. 48H
    b. B5H
    c. B6H
    d. B7H

    Correct Answer: C

    Detailed Solution: The given Chip select corresponds to 101101. For counter 2, A1, A0 will be 10. So, the address of counter 2 would be 10110110 which is nothing but B6H.

19. In order to generate 1 KHz square wave using 8254 operated at 2 MHz clock, the count that must be loaded into counter would be
    a. 03FFH
    b. 07D0H
    c. 1000H
    d. 2000H

    Correct Answer: B

    Detailed Solution: Frequency of the square wave is 1 KHz which corresponds to 1ms. Similarly, Clock time period is 0.5 microsecond. So, the required count would be 1ms/0.5 microsecond, which is equal to 2000. The Hexadecimal equivalent of 2000 is 07D0 H.

20. The hardware-triggered strobe mode of 8254 is same as software-triggered strobe mode except that
    a. Triggering is performed by rising pulse at GATE
    b. Triggering is performed by falling pulse at GATE
    c. Triggering is performed by rising pulse at Clock
    d. Triggering is performed by falling pulse at Clock

    Correct Answer: A

21. Assuming that the interrupt request IR2 has just been serviced in automatic rotation mode, then the next highest priority will be assigned to

a. IR0
b. IR1
c. IR3
d. IR7

Correct Answer: C

Detailed solution: In automatic rotation mode, the interrupt request that has just been serviced is given the lowest priority and the next one is given the highest priority.

22. In automatic end of interrupt,
    a. 8259A resets the highest priority in-service register (ISR) bit
    b. The command specifies which ISR bit to be reset
    c. 8259A resets the lowest priority in-service register (ISR) bit
    d. No command is necessary, during third $\overline{INTA}$ the ISR bit is reset

Correct Answer: D

23. In which of the following modes the ISR does not have information on which IR is being serviced
    a. Nonspecific EOI
    b. Specific EOI
    c. Automatic EOI
    d. None of the above

Correct Answer: C

24. Which of the following is used in cascading mode of 8259A?
    a. ICW 1
    b. ICW 2
    c. ICW 3
    d. ICW 4

Correct Answer: C

25. If the port address of the 8259A for ICW 2 is 81H, then the port address of ICW 3 would be
    a. 80H
    b. 81H
    c. 82H
    d. 83H

Correct Answer: B

Detailed Solution: In both cases A0 = 1. Hence the port address of ICW 3 would be 81H.

26. If the chip select of 8259A is generated using CS = $A7A6A5A4A3A2A1$, then the port address of operation command word OCW 2 would be
    a. 48H
    b. 49H
    c. B6H
    d. B7H

Correct answer: C

Detailed solution: The chip select corresponds to 1011 011 and A0 will be 0. Hence, port address would be 1011 0110 which is B6H.

27. If 16H is loaded into ICW 1 of 8259A, then the 8259A operates in
    a. Single mode with call address interval of 4
    b. Single mode with call address interval of 8
    c. Cascade mode with call address interval of 4
    d. Cascade mode with call address interval of 8

    Correct answer: A

    Detailed solution: 16H corresponds to 0001 0110. The D1 i.e. 2nd LSB is 1 which corresponds to Single mode. Similarly, D2 i.e. 3rd LSB is 1 which corresponds to 4 bytes interval.

28. If 10H is loaded into OCW 1 of 8259A, then
    a. IR2 is masked
    b. IR3 is masked
    c. IR4 is masked
    d. IR5 is masked

    Correct answer: C

29. If 00H is the address of 8237A channel 0 memory address register, then the address of channel 3 count register would be
    a. 01H
    b. 03H
    c. 05H
    d. 07H

    Correct Answer: D

30. The signals AEN and ADSTB of 8237A are used to latch a
    a. Lower order address byte
    b. Higher order address byte
    c. Lower order data byte
    d. Higher order data byte

    Correct answer: B

31. In slave mode DMA controller is treated as
    a. Peripheral
    b. Processor for data transfer from memory to I/O
    c. Processor for data transfer from I/O to memory
    d. Processor for bidirectional data transfer

    Correct answer: A

32. Which of the following statement is FALSE with respect to synchronous serial data transmission?
    a. Transmitter and receiver will be operated by the same clock
    b. Character is transmitted along with the synchronization information
    c. Character is transmitted along with the start and stop bits
    d. Used for high-speed transmission with bit rates more than 20 Kbps

Correct Answer: C

33. In order to transmit ASCII characters in serial bit format at 2000 baud, each bit time duration would be
    a. 0.5 ms
    b. 1 ms
    c. 2 ms
    d. 3.5 ms

    Correct Answer: A

34. In order to convert data bits into audio signals, which of the following is used
    a. Serial to parallel converter
    b. Parallel to serial converter
    c. RS-232C
    d. MODEM

    Correct answer: D

35. The integrated circuit MC 1488 is used to
    a. Convert RS-232C levels into TTL levels
    b. Convert TTL levels into RS-232C levels
    c. Convert RS-232C current levels into RS-232C voltage levels
    d. Convert RS-232C voltage levels into RS-232C current levels

    Correct answer: B

36. The example of full duplex transmission is
    a. Computer to printer
    b. Computer to CRT terminal
    c. Computer to 7-segment display
    d. Computer to computer

    Correct Answer: D

37. If 02H is loaded into 8251A mode word register, which of the following is correct
    a. 8251A operates in synchronous mode
    b. 8251A operates in asynchronous mode with baud rate factor of 1
    c. 8251A operates in asynchronous mode with baud rate factor of 16
    d. 8251A operates in asynchronous mode with baud rate factor of 64

    Correct Answer: C

    Detailed Solution: D1D0=10 in mode word register indicates asynchronous mode with baud rate factor of 16.

38. If the port address of 8251A status register is FFH, the port address of control register would be
    a. FCH
    b. FDH
    c. FEH
    d. FFH

    Correct Answer: D

39. If the transmitter clock frequency of 8251A is 153.6 kHz and the baud rate in asynchronous mode is 2400, the baud rate factor would be
    a. 1
    b. 16
    c. 32
    d. 64

    Correct Answer: D

    Detailed Solution: In asynchronous mode, the baud rate is a fraction of the actual clock frequency. Baud rate factor = Clock frequency/Baud rate

40. The size of display random access memory in 8279 is
    a. 8×8 (B) 16×8 (C) 32×8 (D) 64×8

    Correct Answer: B

    Detailed Solution: Self-explanatory

41. The size of FIFO/Sensor RAM in 8279 is
    (E) 8×8 (F) 16×8 (G) 32×8 (H) 64×8

    Correct Answer: A

EC 8691 - MICROPROCESSOR AND MICROCONTROLLER
(MCQ QUESTIONS WITH ANSWERS)

UNIT 4
8051 MICROCONTROLLER

1. What do you mean by micro in microcontroller?
a) Distance between 2 IC's
b) Distance between 2 transistors
c) Size of a controller
d) Distance between 2 pins

Answer: b
…

2. What is the bit size of the 8051 microcontroller?
a) 8-bit
b) 4-bit
c) 16-bit
d) 32-bit

Answer: a

3. Name the architecture and the instruction set for microcontroller?
a) Van- Neumann Architecture with CISC Instruction Set
b) Harvard Architecture with CISC Instruction Set
c) Van- Neumann Architecture with RISC Instruction Set
d) Harvard Architecture with RISC Instruction Set

Answer: b

4. Number of I/O ports in the 8051 microcontroller?
a) 3 ports
b) 4 ports
c) 5 ports
d) 4 ports with last port having 5 pins

Answer: b

5. Is ROM is used for storing data storage?
a) True

b) False

Answer: b

6. SCON in serial port is used for which operation?
a) Transferring data
b) Receiving data
c) Controlling
d) Controlling and transferring

Answer: c

7. Program counter stores what?
a) Address of before instruction
b) Address of the next instruction
c) Data of the before execution to be executed
d) Data of the execution instruction

Answer: b

8. Auxiliary carry is set during which condition?
a) When carry is generated from D3 to D4
b) When carry is generated from D7
c) When carry is generated from both D3 to D4 and D7
d) When carry is generated at either D3 to D4 or D7

Answer: a

9. What is order of the assembly and running 8051 program?
i) Myfile.asm
ii) Myfile.lst
iii) Myfile.obj
iv) Myfile.hex
a) i,ii,iii,iv
b) ii,iii,I,iv
c) iv,ii,I,iii
d) iii,ii,I,iv

Answer: a.

10. The use of Address Latch Enable is to multiplex address and data memory.
a) True
b) False

Answer: a

11. Which pin provides a reset option in 8051?
a) Pin 1
b) Pin 8
c) Pin 11
d) Pin 9

Answer: d

12. External Access is used to permit _____
a) Peripherals
b) Power supply
c) ALE
d) Memory interfacing

Answer: d

13. What is the address range of SFRs?
a) 80h to feh
b) 00h to ffh
c) 80h to ffh
d) 70h to 80h

Answer: c

14. How many interrupts are there in micro controller?
a) 3
b) 6
c) 4
d) 5

Answer: d

15. Timer 0 is a _____ bit register.
a) 32-bit
b) 8-bit
c) 16-bit
d) 10-bit

Answer: c

16. Number of pins in 8051 microcontroller with _____ package.
a) 40 pin with LLC
b) 60 Pin with QFP
c) 40 pin with DIP
d) 60 pin with QFP

Answer: c

17. Does an 8051 microcontroller need external oscillator to run?
a) True
b) False

Answer: a

18. We use any other frequency source other than crystal oscillator.
a) True
b) False

Answer: a

19. Reset work is _____
a) To make program counter zero but values in registers values are made as zero
b) Program counter is not zero but values in registers values are made as Zero
c) Program counter not zero but values in registers values remain same

d) To make program counter zero but values in registers values remain same

Answer: d

20. What is the minimum no of cycles required for reset operation?
a) 3 cycle
b) 2 cycles
c) 1 cycles
d) 4 cycles

Answer: c

21. PSEN stands for _____
a) Program Select Enable
b) Peripheral Store Enable
c) Program Store Enable
d) Peripheral Select Enable

Answer: c

22. Find the machine cycle for 8051 if XTAL = 11.0592MHz.
a) 90.42us
b) 361.68us
c) 1.085us
d) 150.145us

Answer: b
Explanation: Machine cycle = No.of cycles/frequency
Time = 1/frequency
Time(ns) = 1/11.0592MHz
= 90.42ns
Machine cycles = 12*90.42
= 1.085us.

23. What is the operation for mode 0?
a) 13-bit timer mode, 8-bit timer/counter THx and TLx as 5-bit prescalar
b) 16-bit timer mode, 16-bit timer/counter THx and TLx are cascaded, no prescalar
c) 8-bit auto reload mode, 8-bit auto reload time/counter; THx holds a value

which is to be reloaded into TLx each time it overflows
d) Spilt timer mode

Answer: a

24. What is the operation for mode 1?
a) 13-bit timer mode, 8-bit timer/counter THx and TLx as 5-bit prescalar
b) 16-bit timer mode, 16-bit timer/counter THx and TLx are cascaded, no prescalar
c) 8-bit auto reload mode, 8-bit auto reload time/counter; THx holds a value which is to be reloaded into TLx each time it overflows
d) Spilt timer mode

Answer: b

25. Which is the operation for mode 2?
a) 13-bit timer mode, 8-bit timer/counter THx and TLx as 5-bit prescalar
b) 16-bit timer mode, 16-bit timer/counter THx and TLx are cascaded, no prescalar
c) 8-bit auto reload mode, 8-bit auto reload time/counter; THx holds a value which is to be reloaded into TLx each time it overflows
d) Spilt timer mode

Answer: c

26. Which is the operation for mode 3?
a) 13-bit timer mode, 8-bit timer/counter THx and TLx as 5-bit prescalar
b) 16-bit timer mode, 16-bit timer/counter THx and TLx are cascaded, no prescalar
c) 8-bit auto reload mode, 8-bit auto reload time/counter; THx holds a value which is to be reloaded into TLx each time it overflows
d) Spilt timer mode

Answer: d

27. Function of IE1 in TCON register?
a) External interrupt 1 Edge flag. Not related to timer operations
b) External interrupt 1 Edge flag. Not related to timer operations

c) External interrupt 0 single type control bit
d) External interrupt 1 to be triggered by a falling edge signal

Answer: a

28. 8051 controller contains how many registers?
a) 5
b) 3
c) 1
d) 2

Answer: d

29. General purpose memory is called as _____
a) ROM memory
b) RAM memory
c) SRAM memory
d) EPROM memory

Answer: b

30. Which timer register has both timers in it?
a) TMOD
b) TCON
c) Both TMOD and TCON
d) Neither TMOD nor TCON

Answer: a

31. How many registers can be utilized to write the programs by an effective selection of register bank in program status word (PSW)?
a. 8
b. 16
c. 32
d. 64
ANSWER: (c) 32

32. Which operations are performed by stack pointer during its incremental phase?
a. Push
b. Pop

c. Return
d. All of the above
ANSWER: (a) Push
33) Which is the only register without internal on-chip RAM address in MCS-51?
a. Stack Pointer
b. Program Counter
c. Data Pointer
d. Timer Register
ANSWER: (b) Program Counter

34) What kind of instructions usually affect the program counter?
a.Call & Jump
b. Call & Return
c. Push & Pop
d. Return & Jump
ANSWER: (a) Call & Jump4

35) What is the default value of stack once after the system undergoes the reset condition?
a. 07H
b. 08H
c. 09H
d. 00H
ANSWER:(a) 07H

36) Which bit/s play/s a significant role in the selection of a bank register of Program Status Word (PSW)?
a.RS1
b. RS0
c. Both a & b
d. None of the above
ANSWER: (c) Both a & b

37) Which flags represent the least significant bit (LSB) and most significant bit (MSB) of Program Status Word (PSW) respectively?
a. Parity Flag & Carry Flag
b. Parity Flag & Auxiliary Carry Flag
c. Carry Flag & Overflow Flag
d. Carry Flag & Auxiliary Carry Flag
ANSWER: (a) Parity Flag & Carry Flag

38) Which register bank is supposed to get selected if the values of register bank select bits RS1 & Rs0 are detected to be '1' & '0' respectively?
a.Bank 0
b. Bank 1
c. Bank 2
d. Bank 3
ANSWER: (c) Bank 2

39) It is possible to set the auxiliary carry flag while performing addition or subtraction operations only when the carry exceeds _____
a. 1st bit
b. 2nd bit
c. 3rd bit
d. 4th bit
ANSWER: (c) 3rd bit

40) Which locations of 128 bytes on-chip additional RAM are generally reserved for special functions?
a. 80H to 0FFH
b. 70H to 0FFH
c. 90H to 0FFH
d. 60H to 0FFH
ANSWER: (a) 80H to 0FFH

41) Which commands are used for addressing the off-chip data and associated codes respectively by data pointer?
a. MOVX & MOVC

b. MOVY & MOVB
c. MOVZ & MOVA
d. MOVC & MOVY
ANSWER: (a) MOVX & MOVC
42) Which instruction find its utility in loading the data pointer with 16 bits immediate data?
a. MOV
b. INC
c. DEC
d. ADDC
ANSWER: (a) MOV

43) What is the maximum capability of addressing the off-chip data memory & off-chip program memory in a data pointer?
a. 8K
b. 16K
c. 32K
d. 64K
ANSWER: (d) 64K

44) Which among the below stated registers does not belong to the category of special function registers?
a. TCON & TMOD
b. TH0 & TL0
c. P0 & P1
d. SP & PC
ANSWER: (d) SP & PC

45) What is the required baud rate for an efficient operation of serial port devices in 8051 microcontroller?
a. 1200
b. 2400
c. 4800
d. 9600
ANSWER: (d) 9600

46) Which among the below mentioned functions does not belong to the category of alternate functions usually performed by Port 3 (Pins 10-17)?
a. External Interrupts
b. Internal Interrupts
c. Serial Ports
d. Read / Write Control signals
ANSWER: (b) Internal Interrupts

47) Which output control signal is activated after every six oscillator periods while fetching the external program memory and almost remains high during internal program execution?
a. ALE
b. PSEN
c. EA
d. All of the above
ANSWER: (b) PSEN

48) Which memory allow the execution of instructions till the address limit of 0FFFH especially when the External Access (EA) pin is held high?
a.Internal Program Memory
b. External Program Memory
c. Both a & b
d. None of the above
ANSWER: (a) Internal Program Memory

49) Which signal from CPU has an ability to respond the clocking value of D-flipflop (bit latch) from the internal bus?
a. Write-to-Read Signal
b. Write-to-Latch Signal
c. Read-to-Write Signal
d. Read-to-Latch Signal
ANSWER: (b) Write-to-Latch Signal

50) The upper 128 bytes of an internal data memory from 80H through FFH usually represent _____.
a. general-purpose registers
b. special function registers
c. stack pointers
d. program counters
ANSWER: (b) special function registers

51) What is the bit addressing range of addressable individual bits over the on-chip RAM?
a.00H to FFH
b. 01H to 7FH
c. 00H to 7FH
d. 80H to FFH
ANSWER: (c) 00H to 7FH

52) What is the divisional range of program memory for internal and external memory portions respectively when enable access pin is held high (unity)?
a. 0000H – 0FFFH & 1000H – FFFFH
b. 0000H – 1000H & 0FFFH – FFFFH
c. 0001H – 0FFFH & 01FFH – FFFFH
d. None of the above
ANSWER: (a) 0000H – 0FFFH & 1000H – FFFFH

53) Consider the following statements. Which of them is/are correct in case of program execution related to program memory?
a. External Program memory execution takes place from 1000H through 0FFFFH only when the status of EA pin is high (1)
b. External Program memory execution takes place from 0000H through 0FFFH only when the status of EA pin is low (0)
c. Internal Program execution occurs from 0000H through 0FFFH only when the status of EA pin is held low (0)
d. Internal program memory execution occurs from 0000H through 0FFFH only when EA pin is held high (1)
A & C

b. B & D
c. A & B
d. Only A
ANSWER: (b) B & D

54) How does the processor respond to an occurrence of the interrupt?
a. By Interrupt Service Subroutine
b. By Interrupt Status Subroutine
c. By Interrupt Structure Subroutine
d. By Interrupt System Subroutine
ANSWER: (a) By Interrupt Service Subroutine

55) Which location specify the storage/loading of vector address during the interrupt generation?
a. Stack Pointer
b. Program Counter
c. Data Pointer
d. All of the above
ANSWER: (b) Program Counter

56) Match the following :
a. ISS ——————————— 1. Monitors the status of interrupt pin
b. IER ——————————— 2. Allows the termination of ISS
c. RETI ——————————— 3. MCS-51 Interrupts Initialization
d. INTO ——————————— 4. Occurrence of high to low transition level
A-1, B-2, C-3, D-4
b. A-3, B-2, C-4, D-1
c. A-1, B-3, C-2, D-4
d. A-4, B-3, C-2, D-1
ANSWER:(c) A-1, B-3, C-2, D-4

57) Which among the below mentioned reasons is/are responsible for the generation of Serial Port Interrupt?
a. Overflow of timer/counter 1
b. High to low transition on pin INT1

c. High to low transition on pin INT0
d. Setting of either TI or RI flag
a. A & B
b. Only B
c. C & D
d. Only D
ANSWER: (d) Only D

58) What is the counting rate of a machine cycle in correlation to the oscillator frequency for timers?
1 / 10
b. 1 / 12
c. 1 / 15
d. 1 / 20
ANSWER: (b) 1 / 12

59) Which special function register play a vital role in the timer/counter mode selection process by allocating the bits in it?
a. TMOD
b. TCON
c. SCON
d. PCON
ANSWER:(a) TMOD

60) How many machine cycle/s is/are executed by the counters in 8051 in order to detect '1' to '0' transition at the external pin?
a. One
b. Two
c. Four
d. Eight
ANSWER: (b) Two

61) Which bit must be set in TCON register in order to start the 'Timer 0' while operating in 'Mode 0'?
a. TR0

b. TF0
c. IT0
d. IE0
ANSWER: (a) TR0
62)

62) Consider the below generated program segment for initializing Timer 1 in Mode 1 operation :
MOV SP, # 54 H
MOV TMOD ,# 0010 0000 C
SET C ET1
SETC TR0
SJMP $
a.Which among the below mentioned program segments represent the correct code?
MOV SP, # 54 H
MOV TCON ,# 0010 0000 C
SETC ET1
SETC TR0
SJMP $
b. MOV SP, # 54H
MOV TMOD ,# 0010 0000 C
SETC ET0
SETC TR0
SJMP $
c. MOV SP, # 54 H
MOV TMOD ,# 0010 0000 C
SETC ET1
SETC TR1
SETC EA
SJMP $
d. MOV SP, # 54 H
MOV TMOD ,# 0010 0000 C
SETC ET0
SETC TR1

SETC EA
SJMP $

ANSWER: (c)
MOV SP, # 54 H
MOV TMOD ,# 0010 0000 C
SETC ET1
SETC TR1
SETC EA
SJMP $

63) What is the maximum delay generated by the 12 MHz clock frequency in accordance to an auto-reload mode (Mode 2) operation of the timer?
a. 125 µs
b. 250 µs
c. 256 µs
d. 1200 µs
ANSWER: (c) 256 µs

64) Which among the below mentioned sequence of program instructions represent the correct chronological order for the generation of 2kHz square wave frequency?
MOV TMOD, 0000 0010 B
MOV TL0, # 06H
MOV TH0, # 06H
SETB TR0
CPL p1.0
ORG 0000H
6, 5, 2, 4, 1, 3
b. 6, 1, 3, 2, 4, 5
c. 6, 5, 4, 3, 2, 1
d. 6, 2, 4, 5, 1, 3
ANSWER: (b) 6, 1, 3, 2, 4, 5

65) Why is it not necessary to specify the baud rate to be equal to the number of bits per second?

Because each bit is preceded by a start bit & followed by one stop bit

b. Because each byte is preceded by a start byte & followed by one stop byte

c. Because each byte is preceded by a start bit & followed by one stop bit

d. Because each bit is preceded by a start byte &followed by one stop byte

ANSWER: (c) Because each byte is preceded by a start bit & followed by one stop bit

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(MCQ QUESTIONS WITH ANSWERS)

UNIT 5
INTERFACING MICROCONTROLLER

1. What is the clock source for the timers?
   a) some external crystal applied to the micro-controller for executing the timer
   b) from the crystal applied to the micro-controller
   c) through the software
   d) through programming

   Answer: b

2. What is the frequency of the clock that is being used as the clock source for the timer?
   a) some externally applied frequency f'
   b) controller's crystal frequency f
   c) controller's crystal frequency /12
   d) externally applied frequency/12

   Answer: c
   Explanation: The frequency of the clock source for the timer is equal to f/12(where f is the frequency of the crystal).

3. What is the function of the TMOD register?
   a) TMOD register is used to set various operation modes of timer/counter
   b) TMOD register is used to load the count of the timer
   c) Is the destination or the final register where the result is obtained after the operation of the timer
   d) Is used to interrupt the timer

   Answer: a

4. What is the maximum delay that can be generated with the crystal frequency of 22MHz?
   a) 2978.9 sec
   b) 0.011 msec
   c) 11.63 sec
   d) 2.97 msec

   Answer: d
   Explanation: For generating the maximum delay we have to multiply the maximum number of counts with the time period required to execute one machine cycle(65536*1/22MHz).

5. Auto reload mode is allowed in which mode of the timer?
   a) Mode 0
   b) Mode 1
   c) Mode 2
   d) Mode 3

   Answer: c

6. Find out the roll over value for the timer in Mode 0, Mode 1 and Mode 2?
   a) 00FFH,0FFFH,FFFFH
   b) 1FFFH,0FFFH,FFFFH
   c) 1FFFH,FFFFH,00FFH
   d) 1FFFH,00FFH,FFFFH

   Answer: c
   Explanation: For Mode 0 13 bit value is used so 1FFFH is chosen to be the roll over value. Similarly for Mode 1 FFFFH and for Mode 2 FFH is the roll over value for the timers and counter.

7. What steps are followed when we need to turn on any timer?
   a) load the count, start the timer, keep monitoring it, stop the timer
   b) load the TMOD register, load the count, start the timer, keep monitoring it, stop the timer
   c) load the TMOD register, start the timer, load the count, keep monitoring it, stop the timer
   d) none of the mentioned

   Answer: b

8. If Timer 0 is to be used as a counter, then at what particular pin clock pulse need to be applied?
   a) P3.3
   b) P3.4
   c) P3.5
   d) P3.6

   Answer: b
   Explanation: If Timer 0 is to be used as a counter, then a pulse has to be applied at P3.4 and if it is for Timer 1 then the clock pulse has to be applied at the pin P3.5.

9. In the instruction “MOV TH1,#-3”, what is the value that is being loaded in the TH1 register?
   a) 0xFCH
   b) 0xFBH
   c) 0xFDH
   d) 0xFEH

   Answer: c
   Explanation: Negative value is loaded in 2’s complement form. -3 represented in 2’s complement form as FDH.
   Steps to convert into 2’s complement:

```
3 → 0000 0011          Binary Equivalent of ‘3’
  →  1111 1100         1’s Complement of decimal ‘-3’
  →  1111 1101          2’s Complement of decimal ‘-3’
     F    D           Hex Equivalent of ‘-3’
```

10. TF1, TR1, TF0, TR0 bits are of which register?
    a) TMOD
    b) SCON
    c) TCON

d) SMOD

Answer: c

11. Which of the following best states the reason that why baud rate is mentioned in serial communication?
    a) to know about the no of bits being transmitted per second
    b) to make the two devices compatible with each other, so that the transmission becomes easy and error free
    c) to use Timer 1
    d) for wasting memory

    Answer: b

12. With what frequency UART operates(where f denoted the crystal frequency)?
    a) f/12
    b) f/32
    c) f/144
    d) f/384

    Answer: d
    Explanation: UART frequency is the crystal frequency f/12 divided by 32, that comes out to be f/384.

13. What is the function of the SCON register?
    a) to control SBUF and SMOD registers
    b) to program the start bit, stop bit, and data bits of framing
    c) to control SMOD registers
    d) none of the mentioned

    Answer: b

14. What should be done if we want to double the baud rate?
    a) change a bit of the TMOD register
    b) change a bit of the PCON register
    c) change a bit of the SCON register
    d) change a bit of the SBUF register

    Answer: b
    Explanation: PCON register consists of SMOD bit as its D7 bit, so if we set this bit then the baud rate gets doubled.

15. When an interrupt is enabled, then where does the pointer moves immediately after this interrupt has occurred?
    a) to the next instruction which is to be executed
    b) to the first instruction of ISR
    c) to a fixed location in memory called interrupt vector table
    d) to the end of the program

    Answer: c

16. What are the contents of the IE register, when the interrupt of the memory location 0x00 is caused?
    a) 0xFFH
    b) 0x00H
    c) 0x10H
    d) 0xF0H

    Answer: b
    Explanation: When interrupt of 0x00 is caused (the reset interrupt) then all the other interrupts will be disabled or the contents of the IE register becomes null.

17. After RETI instruction is executed then the pointer will move to which location in the program?
    a) next interrupt of the interrupt vector table
    b) immediate next instruction where interrupt is occurred
    c) next instruction after the RETI in the memory
    d) none of the mentioned

    Answer: b

18. Which pin of the external hardware is said to exhibit INT0 interrupt?
    a) pin no 10
    b) pin no 11
    c) pin no 12
    d) pin no 13

    Answer: c

19. Which bit of the IE register is used to enable TxD/RxD interrupt?
    a) IE.D5
    b) IE.D2
    c) IE.D3
    d) IE.D4

    Answer: d
    Explanation: IE.D4 is used to enable RS interrupt or the serial communication interrupt.

20. Which of the following combination is the best to enable the external hardware interrupt 0 of the IE register (assuming initially all bits of the IE register are zero)?
    a) EX0=1
    b) EA=1
    c) any of the mentioned
    d) EX0=1 & EA=1

    Answer: d

21. Which register is used to make the interrupt level or an edge triggered pulse?
    a) TCON
    b) IE
    c) IPR

d) SCON

Answer: a

22. What is the disadvantage of a level triggered pulse?
    a) a constant pulse is to be maintained for a greater span of time
    b) another interrupt may be generated if the low-level signal is not removed before the ISR is finished
    c) it is difficult to produce
    d) another interrupt may be caused if the signal is still low before the completion of the last instruction

    Answer: d

23. What is the correct order of priority that is set after a controller gets reset?
    a) RI/TI > TF1 > TF0 > INT1 > INT0
    b) RI/TI < TF1 < TF0 < INT1 < INT0
    c) INT0 > TF0 > INT1 > TF1 > RI/TI
    d) INT0 < TF0 < INT1 < TF1 < RI/TI

    Answer: c

24. Why two pins for ground are available in ADC0804?
    a) for controlling the ADCON0 and ADCON1 register of the controller
    b) for controlling the analog and the digital pins of the controller
    c) for both parts of the chip respectively
    d) for isolate analog and digital signal

    Answer: d
    Explanation: Two grounds are available in ADC0804 to isolate analog signal from digital signal. This isolation provides accuracy in digital output.

25. What is the function of the WR pin?
    a) its active high input used to inform ADC0804 to the end of conversion
    b) its active low input used to inform ADC0804 to the end of conversion
    c) its active low input used to inform ADC0804 to the start of conversion
    d) its active high input used to inform ADC0804 to the start of conversion

    Answer: c

26. State which of the following statements are false?
    a) CLK IN pin used for External Clock Input or Internal Clock with external RC element
    b) INTR pin tells about the end of the conversion
    c) ADC0804 IC is an 8 bit parallel ADC in the family of the ADC0800 series
    d) None of the mentioned

    Answer: d

27. While programming the ADC0808/0809 IC what steps are followed?
    a) select the analog channel, start the conversion, monitor the conversion, display the digital results

b) select the analog channel, activate the ALE signal (L to H pulse), start the conversion, monitor the conversion, read the digital results
c) select the analog channel, activate the ALE signal (H to L pulse), start the conversion, monitor the conversion, read the digital results
d) select the channel, start the conversion, end the conversion

Answer: b

28. In ADC0808/0809 IC which pin is used to select Step Size?
a) Vref
b) Vin
c) Vref/2 & Vin
d) None of the mentioned

Answer: a
Explanation: Step Size is calculated by formula Vref/(2^n). As ADC0808/0809 8-bit ADC value of n=8. Therefore formula becomes Vref/(2^8) = Vref/256. If Vref = 5V then Step Size will be 5/256 i.e. 19.53mV.

29. What is the difference between ADC0804 and MAX1112?
a) ADC0804 has 8 bits and MAX1112 has 1 bit for data output
b) ADC0804 is used for adc and dac conversions whereas MAX1112 is used for serial data transmissions
c) ADC0804 has 32 bits and MAX1112 has 3 bit for data output
d) None of the mentioned

Answer: a
Explanation: ADC0804 is used for parallel ADC and MAX1112 is used for serial ADC.

30. Which of the following statements are true about DAC0808?
a) parallel digital data to analog data conversion
b) it has current as an output
c) all of the mentioned
d) none of the mentioned

Answer: a

31. 8 input DAC has _____
a) 8 discrete voltage levels
b) 64 discrete voltage levels
c) 124 discrete voltage levels
d) 256 discrete voltage levels

Answer: d
Explanation: For n input DAC has 2^n discrete voltage levels.

32. INTR, WR signal is an input/output signal pin?
a) both are output
b) both are input
c) one is input and the other is output

d) none of the mentioned

Answer: c
Explanation: INTR pin tells about the end of the conversion (output) and WR pin tells us to start the conversion (input).

33. What is the difference between LM 34 and LM 35 sensors?
    a) one is a sensor and the other is a transducer
    b) one's output voltage corresponds to the Fahrenheit temperature and the other corresponds to the Celsius temperature
    c) one is of low precision and the other is of higher precision
    d) one requires external calibration and the other doesn't require it

    Answer: b
    Explanation: LM 34's output voltage corresponds to the Fahrenheit temperature and LM 35 corresponds to the Celsius temperature.

34. What is signal conditioning?
    a) to analyse any signal
    b) conversion or modification is referred to as conditioning
    c) conversion from analog to digital is signal conditioning
    d) conversion from digital to analog is signal conditioning

    Answer: b.

35. What steps have to be followed for interfacing a sensor to a microcontroller 8051?
    a) make the appropriate connections with the controller, ADC conversion, analyse the results
    b) interface sensor with ADC and ADC with 8051
    c) interface sensor with the MAX232, send now to microcontroller, analyse the results
    d) none of the mentioned

    Answer: b.

36. LM35 has how many pins?
    a) 2
    b) 1
    c) 3
    d) 4

    Answer: c
    Explanation: LM35 has 3 pins.
    1.Power(+5 Volts)
    2.Output analog voltage
    3.Ground(0 Volts)

37. Why Vref is set of ADC0848 to 2.56 V if analog input is connected to the LM35?
    a) to set the step size of the sampled input
    b) to set the ground for the chip
    c) to provide supply to the chip

d) all of the mentioned

Answer: a
Explanation: Vref is used to set the step size of the ADC conversion, if it is selected to 2.56 then the step size will be selected to 10mV, so for every step increase of the analog voltage an increase of 10 mV will be there.

38. Which of the following steps detects the key in a 4*4 keyboard matrix about the key that is being pressed?
a) masking of bits
b) ensuring that initially, all keys are open
c) checking that whether the key is actually pressed or not
d) all of the mentioned

Answer: d
Explanation: For detecting that whether the key is actually pressed or not, firstly this must be ensured that initially all the keys are closed. Then we need to mask the bits individually to detect that which key is pressed. Then we need to check that is the key actually pressed or not, by checking that whether the key pressed for a time more than 20 micro seconds.

39. What is described by this command: CJNE A,#00001111b, ROW1
a) it masks the bit and then jumps to the label where ROW1 is written
b) it makes the value of the accumulator 0FH and then jumps at the address where ROW1 label is written
c) it compares the value of the accumulator with 0FH and jumps to the location where ROW1 label is there if the value becomes equal
d) it compares the value of the accumulator with 0FH and jumps to the location where ROW1 label is there if the value is not equal

Answer: d
Explanation: This particular command CJNE A,#00001111b, ROW1 compares the value of the accumulator with OFH and jumps to ROW1 address if the value is not equal.

40. To detect that in which column, the key is placed?
a) we can mask the bits and then check it
b) we can rotate the bits and then check that particular bit which is set or reset(according to the particular condition)
c) none of the mentioned
d) all of the mentioned

Answer: d

41. In reading the columns of a matrix, if no key is pressed we should get all in binary notation
a) 0
b) 1
c) F
d) 7

Answer: b
Explanation: If no key is pressed, then all the keys show 1 as they are all connected to power supply.

42. If we need to operate a key of a keyboard in an interrupt mode, then it will generate what kind of interrupt?
    a) ES
    b) EX0/EX1
    c) T0/T1
    d) RESET

    Answer: b
    Explanation: If a key is to operate in an interrupt mode then it will generate an external hardware interrupt.

43. To identify that which key is being pressed, we need to:
    a) ground all the pins of the port at a time
    b) ground pins of the port one at a time
    c) connect all the pins of the port to the main supply at a time
    d) none of the mentioned

    Answer: b
    Explanation: To detect that which key is being pressed, we need to ground the pins one by one.

44. Key press detection and Key identification are:
    a) the same processes
    b) two different works are done in Keyboard Interfacing
    c) none of the mentioned
    d) any of the mentioned

    Answer: b
    Explanation: They are two different works that are involved in Keyboard Interfacing. One is used for checking that which key is being actually pressed and the other is used to check that is the key actually pressed or not.

45. Why do we need a ULN2803 in driving a relay?
    a) for switching a motor
    b) for increasing the current
    c) for increasing the power
    d) for switching the voltage

    Answer: b
    Explanation: We need a ULN2803 for driving a relay because the relay coil requires 10mA or more current to be energized. If microcontroller pins are not able to provide sufficient current to drive relays then we need ULN2803 for driving relays.

46. How can we control the speed of a stepper motor?
    a) by controlling its switching rate
    b) by controlling its torque
    c) by controlling its wave drive 4 step sequence

d) cant be controlled

Answer: a
Explanation: Speed of a stepper motor can be controlled by changing its switching speed or by changing the length of the time delay loop.

47. How many rows and columns are present in a 16*2 alphanumeric LCD?
    a) rows=2, columns=32
    b) rows=16, columns=2
    c) rows=16, columns=16
    d) rows=2, columns=16

    Answer: d

48. How many data lines are there in a 16*2 alphanumeric LCD?
    a) 16
    b) 8
    c) 1
    d) 0

    Answer: b

49. Which pin of the LCD is used for adjusting its contrast?
    a) pin no 1
    b) pin no 2
    c) pin no 3
    d) pin no 4

    Answer: c
    Explanation: Pin no 3 is used for controlling the contrast of the LCD.

50. For writing commands on an LCD, RS bit is
    a) set
    b) reset
    c) set & reset
    d) none of the mentioned

    Answer: b

51. Which command of an LCD is used to shift the entire display to the right?
    a) 0x1C
    b) 0x18
    c) 0x05
    d) 0x07

    Answer: a

52. Which command is used to select the 2 lines and 5*7 matrix of an LCD?
    a) 0x01
    b) 0x06
    c) 0x0e

d) 0x38

Answer: d

53. Which of the following step/s is/are correct for sending data to an LCD?
    a) set the R/W bit
    b) set the E bit
    c) set the RS bit
    d) all of the mentioned

    Answer: d
    Explanation: To send data to an LCD, RS pin should be set so that LCD will come to know that it will receive data which has to display on the screen. R/W pin should be reset as data has to be displayed (i.e. write to the LCD). High to low pulse must be applied to the E pin when data is supplied to data pins of the LCD.

54. Which of the following step/s is/are correct to perform reading operation from an LCD?
    a) low to high pulse at E pin
    b) R/W pin is set high
    c) low to high pulse at E pin & R/W pin is set high
    d) none of the mentioned

    Answer: c

55. Which instruction is used to select the first row first column of an LCD?
    a) 0x08
    b) 0x0c
    c) 0x80
    d) 0xc0

    Answer: c